Future Directions Workshop: Materials, Processes, and R&D Challenges in Microelectronics

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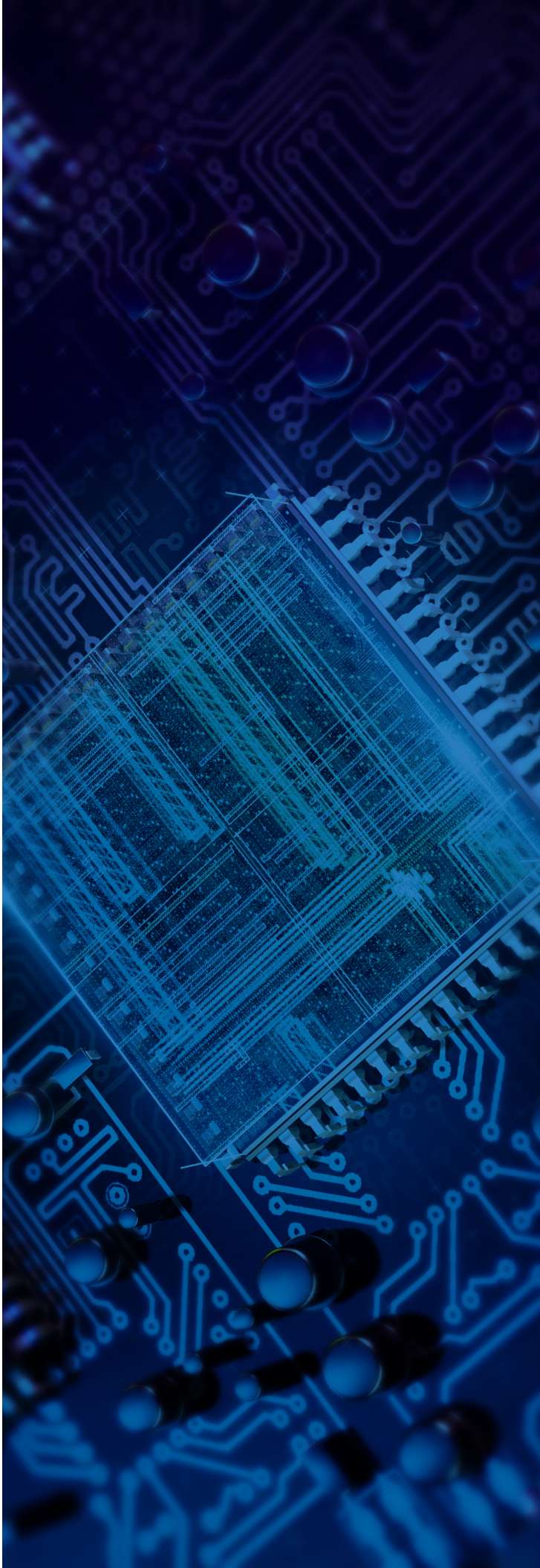

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Innovation is the key to the future, but basic research is the key to future innovation.

–Jerome Isaac Friedman,
Nobel Prize Recipient (1990)

Preface

Over the past century, science and technology has brought remarkable new capabilities to all sectors of the economy; from telecommunications, energy, and electronics to medicine, transportation and defense. Technologies that were fantasy decades ago, such as the internet and mobile devices, now inform the way we live, work, and interact with our environment. Key to this technological progress is the capacity of the global basic research community to create new knowledge and to develop new insights in science, technology, and engineering. Understanding the trajectories of this fundamental research, within the context of global challenges, empowers stakeholders to identify and seize potential opportunities.

The Future Directions Workshop series, sponsored by the Basic Research Directorate of the Office of the Under Secretary of Defense for Research and Engineering, seeks to examine emerging research and engineering areas that are most likely to transform future technology capabilities. These workshops gather distinguished academic researchers from around the globe to engage in an interactive dialogue about the promises and challenges of each emerging basic research area and how they could impact future capabilities. Chaired by leaders in the field, these workshops encourage unfettered considerations of the prospects of fundamental science areas from the most talented minds in the research community.

Reports from the Future Direction Workshop series capture these discussions and therefore play a vital role in the discussion of basic research priorities. In each report, participants are challenged to address the following important questions:

- How will the research impact science and technology capabilities of the future?
- What is the trajectory of scientific achievement over the next few decades?
- What are the most fundamental challenges to progress?

This report is the product of a workshop held June 23-24, 2022, at the Basic Research Innovation Collaboration Center in Arlington, VA on the future of Microelectronics research. It is intended as a resource to the S&T community including the broader federal funding community, federal laboratories, domestic industrial base, and academia.

Executive Summary

Microelectronics is a complex field with ever-evolving technologies and business needs, fueled by decades of continued fundamental materials science and engineering advancement. Decades of dimensional scaling have led to the point where even the name "microelectronics" inadequately describes the field, as most modern devices operate on the nanometer scale. As we reach physical limits and seek more efficient ways for computing, research in new materials may offer alternative design approaches that involve much more than electron transport (e.g. photonics, spintronics, topological materials, and a variety of exotic quasi-particles). New engineering processes and capabilities offer the means to take advantage of new materials designs (e.g. 3D integration, atomic scale fabrication processes and metrologies, digital twins for semiconductor processes and microarchitectures). The wide range of potential technological approaches provides both opportunities and challenges.

The Materials, Processes, and R&D Challenges in Microelectronics Future Directions workshop was held June 23-24, 2022, at the Basic Research Innovation Collaboration Center in Arlington, VA, to examine these opportunities and challenges. Sponsored by the Basic Research Directorate of the Office of the Under Secretary of Defense for Research and Engineering, it is intended as a resource for the S&T community including the broader federal funding community, federal laboratories, domestic industrial base, and academia.

The workshop was divided into three key areas of microelectronics:

- **Conventional Computing:** pushing the envelope on state-of-the-art computing systems (von Neumann architecture), with separated memory and processing, and where innovation has largely been driven to-date by scaling (Moore's law).
- **Unconventional Computing:** new architectures that enable new workloads and extreme improvements in power efficiencies (i.e., in-memory and in-sensor computing, neuromorphic computing, quantum, and analog accelerators within digital computing environments)
- **Power/High Frequency Electronics:** materials and device physics that may enable active and passive components for future compact and efficient electronics in power distribution, wireless, automotive, and space environments.

Research Challenges & Opportunities

The workshop participants identified the following key challenges and opportunities for these three areas:

Conventional Computing

- **Logic Devices:** Breakthrough improvements will result from transistors being able to deliver two characteristics that are not possible today: extreme low voltage switching without increase of variability, off currents, and loss of gain; and the ability to do complementary metal-oxide-semiconductor on polycrystalline or amorphous transistors so these transistors can be fabricated at low temperatures and layered in monolithic 3D chips with performance characteristics that are comparable to single crystal silicon transistors today.
- **Memory:** The near-perfect memory, one that is low power, as fast as SRAM, and as dense as DRAM and FLASH, and preferably with on-chip capability, does not yet exist. Identifying the materials and physics that would create such a memory is a grand challenge that would revolutionize computing.
- **Heterogeneous Integration:** The vision for heterogeneous integration is to be able to fuse the differences between the chip and the package while significantly improving functionality. Additionally, future heterogeneous integration desires the ability to create bespoke systems by mixing and matching chips and components from a set of common components and standardized interconnect links.
- **Atom-scale Direct Write, 3D Nanofabrication and Metrology:** The recent demonstrations of NAND Flash memories with 232 layers vertically stacked is a tour de force, custom engineered for a very specific device structure. This 3D stacking method may not be generally applicable to a large variety of devices. Additionally, today, current lithography techniques are limited to ~ 8 nm at scale by line edge roughness and device doping processes suffer uncertainties in implant resolutions due to stochasticity. These restrictions in today's lithography driven nanofabrication sets atomic scale precision in fabrication as a challenge for the future.
- **Need for New Three-Dimensional Materials Characterization Techniques:** The need for the future is in measuring three dimensional structures, preferably in a minimally disruptive manner, with atomic level chemical and structural resolution, and with rapid throughput for the next generation of microelectronics progress.
- **Need for New Thermal Materials and Understanding:** Within the current paradigm of microelectronic systems, the overarching limitation here is heat removal from three dimensional heterogeneous structures. Solving this issue calls for discovering new high thermal conductivity engineered materials and physics-based approaches for heat removal for innovations in new thermal materials and approaches.
- **Processing Science:** At a fundamental level, we need to further understand deposition and etching and their reaction pathways. We will need to develop low temperature processing capabilities that enable many different materials to be integrated together.

Unconventional Computing

- **The Need for Co-Design:** In computing, co-design continues to be the key to future advancements, but as new ways to compute are developed, we can leverage unique materials properties in smartly designed devices that are correctly fabricated to achieve system-level benefits.

- **The Compute-Energy Bottleneck:** A main issue is the memory bottleneck in von Neumann architectures, where the computing energy and execution time is severely limited by memory access, caused by a combination of interconnect delay memory latency, and above all, bandwidth.
- **Connecting Across the Analog-to-Digital Interface in Computing:** The analog-to-digital-conversion bottleneck is especially apparent in two areas. The first is in edge computing devices where the computer interacts with sensors in the real world, needs to process the data, and then send the data to the cloud. The second is for future computing designs where an analog accelerator will be embedded within a digital CMOS computing ecosystem, and therefore needs an analog-to-digital interface.
- **Hybrid Systems Classical/Quantum Systems:** We can think of such systems as accelerators that are embedded within classical computing ecosystems. The hardware and software challenges lie in the interfacing with such accelerators.
- **Variability and Error Tolerance in Low-Energy Processes:** Any unconventional approach that departs from digital logic needs to deal with the potential propagation and amplification of errors in a large computing system. Secondly, in keeping with the needs for low-energy computing, any new approaches will need to rely on low-energy physical or chemical processes. These can increase device variability, leading to errors. Promising unconventional computing solutions are ones that can achieve system-level metrics or goals, even with errors present (i.e. error tolerant).

Power/High-Frequency Electronics

- **Platform for Heterogenous Integration:** exploring with basic and fundamental research towards integrating emerging semiconductors with magnetics, heat spreaders, dielectric materials, and other semiconductors for functionalities.
- **Thermal Management:** This area requires fundamental research on the synthesis, characterization, and modeling of thermal materials performance. This includes the measurement and analysis of thermal conductivities, thermal boundary resistances, integration of thermal materials, as well as theory and modeling of phonon transport in three dimensional heterostructures consisting of semiconductors, dielectrics, and metals.
- **Bulk Growth:** Availability of low-cost, small-diameter substrates prior to scaling is a major challenge that slows the pace of research. Some of the important materials for which bulk crystal substrate development is important are aluminum nitride, boron nitride, diamond, III-oxides.
- **Epitaxial Growth:** It is important to focus on the development of epitaxial heterostructures and their control for these new materials for high-power and high-frequency applications, in the same manner that epitaxial Gallium Nitride and Silicon Carbide materials development. New theoretical understanding and accurate models are required for being able to accurately predict the properties of epitaxial films grown under non-equilibrium conditions.
- **Dielectric Materials:** ultra-wide bandgap materials require dielectric materials with high-K, appropriate conduction band offsets, and breakdown electric field strengths. This implies fundamental research of the synthesis and integration of dielectric materials in combination with the semiconductor material synthesis/growth/fabrication.
- **Dopant and Defect Studies:** With the needed expansion of the bandgap, the incorporation, activation, and compensation of both dopants and defects are not clearly understood. This can stall the development cycle of the new semiconductors, and if overlooked, can lead to major disruptions later down the line.
- **Magnetic, Piezoelectric, and Ferroelectric Materials:** Synthesis and integration of piezoelectric and ferroelectric materials, as well as their characterization, charge transport, theory, and experimental set up to characterize and model their high field behavior is needed.
- **Science of Processing and Characterization:** Since the set of materials for active and passive components are emerging, this is a key area recognized by the panel as a research opportunity. Areas under this heading include ultra-high-pressure annealing, etching with new chemistry, high-temperature activation processes, radiation tolerance, and high-temperature behavior.
- **Reliability Science:** Better scientific understanding of failure modes and their analysis in semiconductors is needed at earlier stages of development. Innovative tools (physical and theoretical) that give us an early look into the physics of degradation and failures at the device level are needed. This will help to predict a material's full potential accurately and in a timely manner.

Research Trajectory

Information processing machines, driven by microelectronics, have enabled the global computing and communication revolutions and the information age. Over the next three decades, its impact will expand to new technologies that will change the way we live and work around the globe. These will include autonomous vehicles, automation and robotics, efficient electrical power distribution, global communication networks, managing climate change, food production, and national security. Given the foundational nature of microelectronics to all modern computation and communications technologies, workshop participants identified the following research trajectory needed to underwrite this anticipated progress.

- Furthering the physics, chemistry, and computational science of microelectronic materials for fast and accurate predictability.
- Atom-scale, deterministic nanofabrication in three dimensions
- The physics of carrier and thermal transport in multi-scale and imperfect heterogeneous media
- Three-dimensional material characterization with chemical and physical resolution at atomic scale
- The science of reliability, resiliency, and adapting to the presence of noise and defects

- Unconventional computing approaches with a co-design perspective
- Heterogeneous integration
- Discovery science of new functional and scalable materials for high-power microelectronics components

The workshop participants identified key enablers to realizing the projected research trajectory which include: targeted and coordinated infrastructure, risk management, and broader engagement with the larger research community.

For the infrastructure enablers, these could be in the form of centers under one roof, or there could be other alternatives. Such capabilities would uniquely provide the materials synthesis and measurement infrastructure, teams (academia and industry), and modus operandi for research required to maximize the chances of impact. We describe some of these infrastructure needs below.

- Capability for atomic scale 3D nanofabrication and process science
- Science for next-generation microelectronic devices and their heterogeneous integration
- Capability for the discovery science of new materials for heterogeneous microelectronics
- Capability for co-design of future computation systems

In conclusion, the consensus of the workshop participants is that we are at a crossroads. They agree that if research and development proceed along the current trajectory, future progress in energy efficiency and cost/compute reductions will be limited by the laws of physics. An alternative path to overcome these limitations will need the theoretical and experimental exploration of new materials; new ways of fabricating and putting together components in three dimensions and at atomic scales; and the exploration of new computing architectures and new devices that can offer orders of magnitude improvement in performance, energy consumption and cost. The workshop participants believe this is possible with an emphasis on fundamental basic research, complemented with engineering research that informs and builds upon the basic science discoveries.

Introduction

Information processing machines, driven by microelectronics, have enabled the global computing and communication revolutions and the information age. Over the next three decades its impact will expand to new technologies that will change the way we live and work around the globe. These will include autonomous vehicles, automation and robotics, efficient electrical power distribution, global communication networks, managing climate change, food production, and national security. Given the foundational nature of microelectronics to all modern computation and communications technologies, what are the developments in microelectronics science that would be needed to underwrite this anticipated progress?

To examine this, first let us envision an information processing machine 20+ years out into the future. Today's mostly von Neumann computing environment will integrate with increasingly larger numbers of embedded accelerators providing extreme power efficiency, tamper proof security, and—with additional classical, neuromorphic, and quantum information-based processors—the ability to solve problems unsolvable today. Whether computing's centroid will remain around a von Neumann architecture or whether that balance will shift, it is too early to say. The accelerators may employ a variety of computing paradigms: some of them may be biologically inspired or based on quantum information science. These processors will blur the distinction between memory and compute, and they will significantly eliminate the need for data transport along electrical connections, reducing energy consumption. When energetically efficient data transport is needed over long distance, photon-based communications will be seamlessly integrated with the electronic systems. Computing will be both centralized, as well as distributed (at the edge, or next to sensors) to enable fast, fully autonomous system that are currently limited by the latencies of cloud-based processing. The energy per compute operation will scale down by a factor of ~1000 (assuming historical trends of GPU energy efficiency doubling every two years continues) and the speed of high-performance computing will target the zetaflop range. The cost for computing will target a >100X reduction in processing speed per dollar over the next twenty years[1]. Such systems will couple to human-computer interfaces with capabilities far beyond what exists today. In 25 years, they will possibly weigh 10 grams or less, and have >20 hours of battery life, with capabilities far beyond what is possible with today's virtual reality/augmented reality headsets. We would not have to worry about the ephemerality of power availability to our mobile systems. This is the progress that will be needed for information processing to continue its historic trend for revolutionary global impact and will require significant progress in microelectronics science. We discuss this below.

On a more granular level, our progress will be increasingly informed by an understanding of how biological information processing works and the understanding of quantum coherent systems and quantum phenomena, and/or non-linear phenomena and material physics at micro- and nano-scales. These vast hitherto unexplored areas will fuel future advances. Chip topologies will be three-dimensional instead of two, in order to provide the large number and variety of devices needed for an energy-efficient system. We would need to determine how to make faster and cheaper memory and integrate multiple processors and memory chiplets with ultra-fast data connection pathways at high densities and on the same substrate, without loss in energy efficiency and speed. Just as we can today swap out server boxes in a data center, designers and companies should be able to plug-and-play with processor chiplets made by different manufacturers to design our own high-performance systems. We would be able to send power in and pull heat out of three-dimensional chips where now heat is produced within embedded volumes, increasing the challenges for its transport and rejection. Our semiconductor manufacturing fabs would be well within the mandates of the Paris Accord of cutting total emissions in half every decade, a challenge considering the continued growth of the semiconductor industry (Ragnarsson et al., 2022). We will be able to create virtual models of the entire semiconductor manufacturing process flow, leading to development of fabrication processes using very little trial and error, and near dead reckoning of performance using accurate simulation models.

At a hardware level, this will require innovation spanning multiple disciplines. This includes mixed-signal processing of data at sensor nodes; new, neuro-informed information extraction and interpretation; data storage that is dense, low-power, and low-leakage; understanding quantum-classical hybrid interfaces; efficient and multi-modal communication; embedded intelligence; intrinsic security; and small form-factor packaging, as well as other technical and scientific challenges, still to be discovered.

For the past 50 years, the development of microelectronics technology has been akin to walking inside a well-lit tunnel. The way ahead was clear as there was a well-defined path—which involved the two-dimensional (2D) shrinking of devices (transistors, memory, and wires) to pack more components in the same chip area—that everyone diligently followed. Today, as we are hitting the physical limits of this 2D scaling, we are also approaching the exit of the tunnel. Beyond, new paths lie ahead for microelectronics made possible by innovations from materials to architecture. It is imperative that these new paths be discovered and developed for the continued progress of the information age.

The physical science progress required to enable this future microelectronics technology is challenging, yet realistic and intellectually inspiring. It will require, for example, a deeper

1 This number (measured in MIPS/dollar and Flops/dollar by different workers) has reduced by an order of magnitude approximately every 5 years since 1940, slowing to every 10-16 years in the 2010s (for an assessment see (AI Impacts, 2015, 2018) and references therein).

understanding of the physics of electronic and thermal transport in heterogeneous systems at the nanoscale. It will also require the continued exploration of the physics of spin, phonons, and topological systems. Because it is fundamentally impossible to deterministically control every atom, future nanosystems will require new ways of handling defects, in addition to developing ways to deterministically place and pattern at atomic, rather than at nanometer length scales. Besides, these methods will be different from today's methods because we need to build structures in three dimensions rather than two. This will require us to design and synthesize a host of new semiconducting, dielectric, metallic, and piezo/ferroelectric materials for logic, memory and thermal transport that can meet several performance criteria in parallel. Time is also part of the design efficiency equation. Dynamical (in time) and reconfigurable hardware will be discussed later.

Rather than rely solely on silicon-based devices and metal wires to perform all desired functions, we must use heterogeneous materials and customized device structures optimally designed to perform diverse and distinct functions—i.e., domain-specific device technology. This includes functions in addition to compute and memory/storage: such as sensor/actuators, radio frequency/high-frequency and wireless communication, high-power and high voltage devices for power management and delivery, light sources, detectors, and wave guides for communication. Discovery of new materials will need to progress much faster than the trial-and-error methods we use today. These discoveries will not only rely on curiosity, but will also be guided by co-design[2] across abstraction boundaries from system architecture, to circuits and devices, processing technology and fundamental materials science that support the abstraction layers above. These new designs will push hard on the material set and fabrication processes we are comfortable using today. Because of this departure from the status quo, we will need to reemphasize processing science. Finally, we will require major progress in the theoretical understanding of material behavior, stability and property prediction under equilibrium and non-equilibrium situations so that we will be able to predict, with a high degree of confidence, performance of materials that are possibly imperfect, without experimental trial and error.

The focus of this workshop was to identify the basic materials and processing science research needs that would support and impact the continued progress of microelectronics to meet the needs described earlier. Two days of intense discussion, facilitated by a pre-workshop survey and lead-in talks by industry experts, identified many fruitful paths going forward. This report is organized around eight major research trajectories that address research challenges and opportunities in three key areas: conventional computing, unconventional computing, and power/high-frequency electronics (Figure 1).

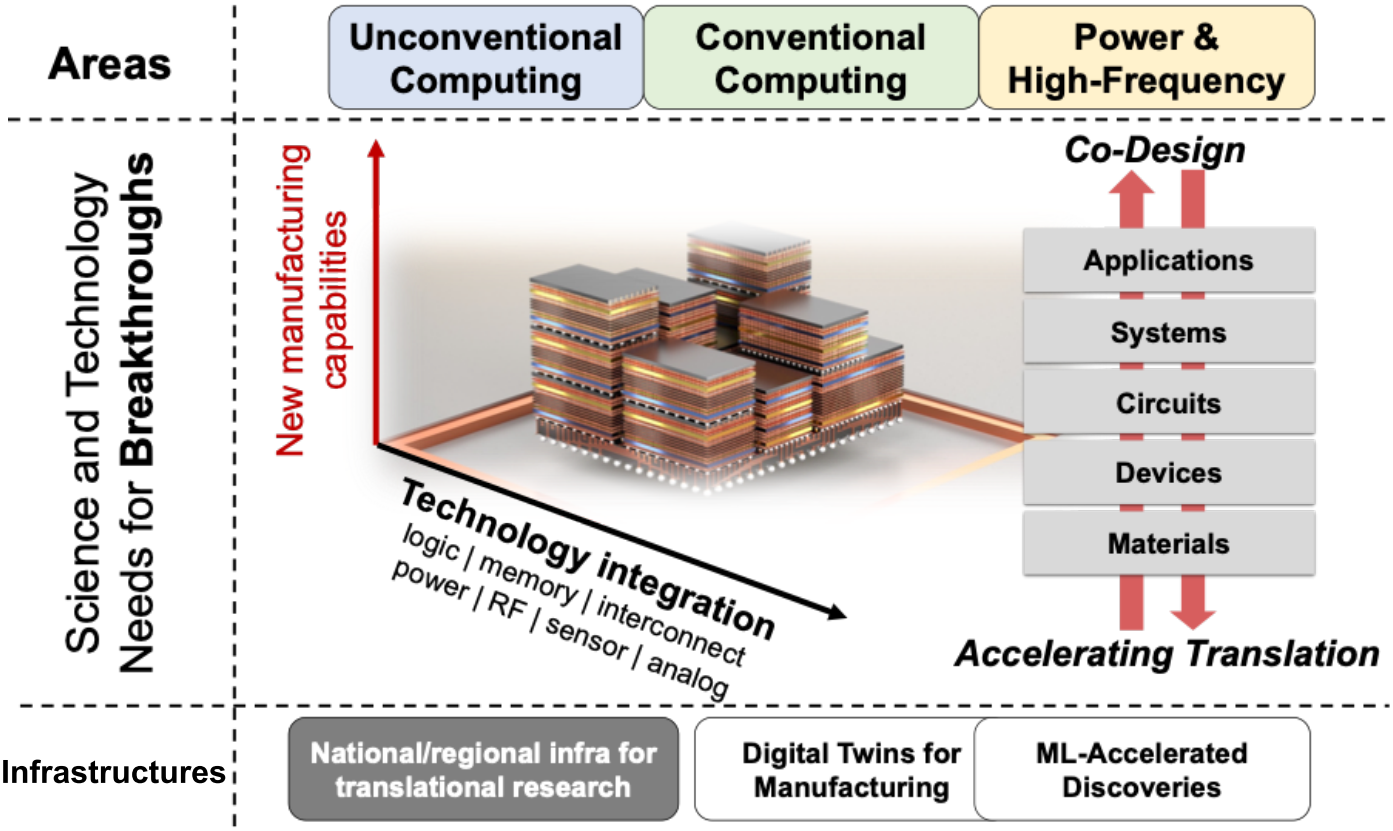

Figure 1The needs for science and technology breakthroughs in unconventional, conventional computing, and power and high-frequency are identified. Three major infrastructures have been identified to accelerate the growth and development in the three areas.

2 https://science.osti.gov/-/media/bes/pdf/reports/2019/BRN_Microelectronics_rpt.pdf

Research Challenges & Opportunities

In this section we describe the key problem set, challenges and technical hurdles for microelectronics, and the materials research opportunities that arise from it. Note that because the potential technologies go beyond the standard definition of electronic physics (transport, classical electromagnetics), "microelectronics" should be viewed in a much broader sense. This section is divided into three areas: conventional computing, unconventional computing, and high-power electronics. Note that there is considerable overlap between these areas and therefore this demarcation should not be taken as too rigid. Considerations that have already appeared in conventional computing, for instance, may be relevant for unconventional computing and high-power, however they are not repeated in those sections. A note on the distinction between "conventional" and "unconventional" computing: conventional computing generally covers the area of the established von Neumann architecture, with separated memory and processing, and where innovation has largely been driven to-date by scaling (Moore's law). Unconventional computing generally covers the area of new materials, devices, circuits, and architectures outside of this von Neumann paradigm. Naturally, as technologies mature, the line between these two definitions can become blurred.

Conventional Computing

Here we discuss microelectronics activities that pertain to computing within the current von Neumann architecture framework. For many years conventional computing was largely driven by transistor scaling. The advent of two materials-driven breakthroughs in the construction of the transistor: (i), the use of hafnium oxide-based dielectrics and a metal gate (2007); and (ii), the transition from planar to three-dimensional transistors (Samsung, 2022) led to improvements in electrostatic control, scaling, and current drive; ultimately enabling the current 5nm technology node that is in production. As will be discussed later in this section, the future challenge for the transistor is to be able to deliver an order of magnitude or more reduction in operating voltage (0.7 V) and operation energies than what is possible today (Theis & Wong, 2017). Today, the bottleneck for conventional computing is in communication between the compute and the memory of the machine, and in the availability of cheap, fast, dense, and readily addressable memory that can be incorporated on-chip and off-chip. For over a decade, progress in the computing throughput has been faster than the memory bandwidth, i.e. the execution of logic computation has been progressing faster than that rate at which data can be transported to and from memory (DACTv, 2022). Therefore, materials and process breakthroughs in new types of communications and memories that are energy efficient, low footprint, and cheap by at least an order-of-magnitude will be key to driving the next breakthroughs in conventional computing. Not only this, but the progress needs to be fast enough to meet needs—for instance, the current rate of increase in energy efficiency is ~ 2X every 2 years (Liu, 2021). To even maintain this rate of increase would call for significant shifts in the materials and approaches that we will need, and it will engage a significant amount of discovery science of a fundamental nature. We discuss some of the key considerations for conventional computing, relevant to basic materials and process research below and illustrated in Figure 2.

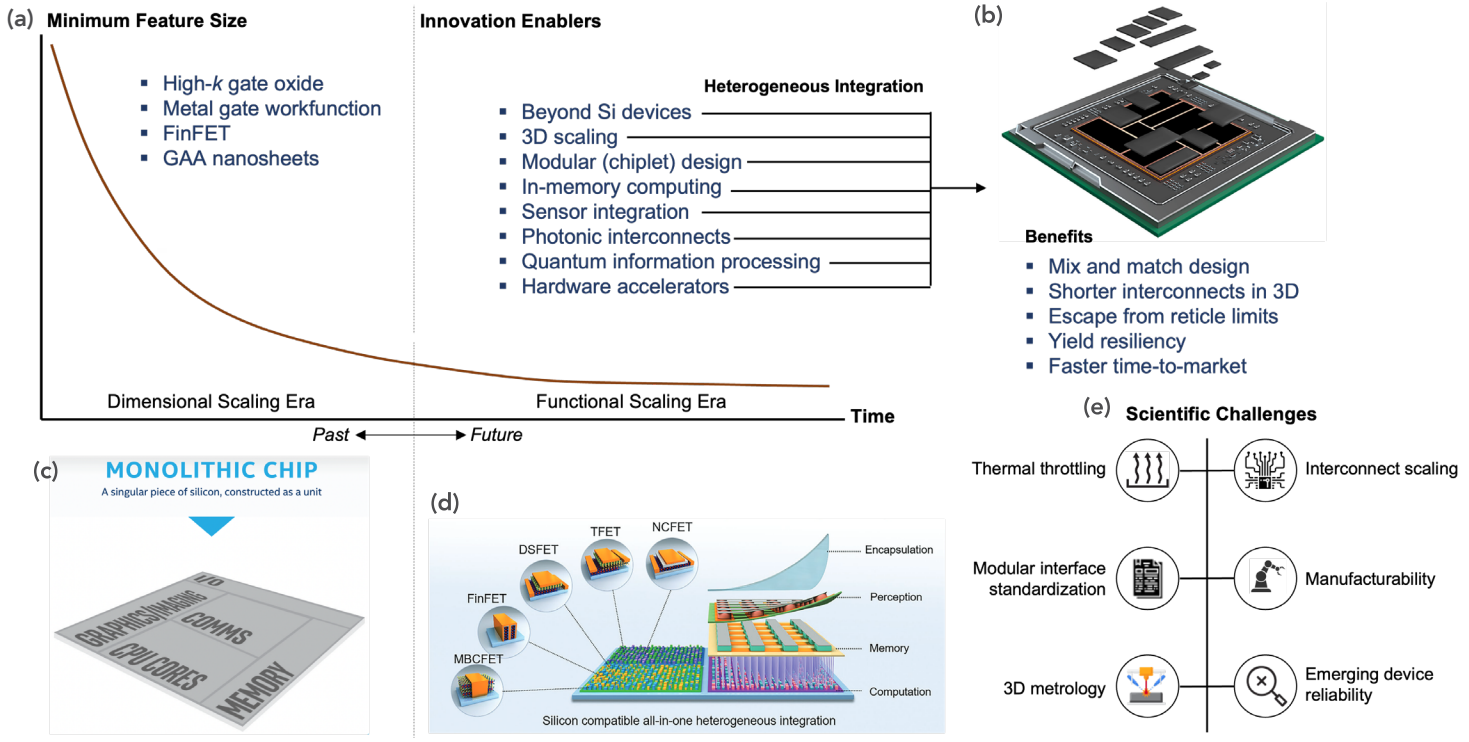

Figure 2 The future of Conventional Computing will be served mainly through functional scaling (a), led by efficient heterogenous integration (b) and (c), using novel 3D scaled transistor structures (d) that supersedes 2D scaling. The innovation enablers and science challenges are identified (e). [Adapted from (Park, 2020); (Wang et al., 2022)]

Logic Devices

For logic devices, breakthrough improvements will result from transistors being able to deliver two characteristics that are not possible today. The first is extreme low voltage switching (current switching voltages are ~ 0.7 V; a viable target is ~300 mV) without increase of variability, off currents, and loss of gain. The second is being able to do complementary metal-oxide-semiconductor (CMOS) on polycrystalline or amorphous transistors with performance characteristics that are comparable to single crystal silicon transistors today. Overcoming this challenge will be a paradigm shift: it will lift the longstanding and restrictive dependency on silicon single crystal devices. Good CMOS circuits can only be built using single crystal n and p metal-oxide-semiconductor field-effect transistors (MOSFET) that are monolithically built on a single crystal wafer. This advance would enable logic circuitry to be stacked upon memory circuitry, as well as the interconnect back-end, leading to extensive flexibility in hardware design. These device layers could then be scalable to multiple such layers—essentially a three-dimensional high rise with logic and memory floors that can be freely interspersed. Achieving this will most likely require new materials that are not silicon, and both will require a systematic discovery science effort for materials, property measurement and their prediction, rather than a scattershot approach. Low voltage switching will require radically new approaches that may need to exploit as-yet unexplored physics: such as new states of switching between different ground states, and novel state variables such as atomic orbitals and magnetic texture. For charge-based device approaches, it will require engineered materials with high density of states, low effective masses, high maximum electron densities and high Fermi velocities—leading to increased channel velocities without compromising on/off currents. Any work on low voltage devices must account for the entire system i.e., developing low voltage devices is a necessary but not a sufficient condition. This has been a shortcoming of past research in this area. We need to look at the entire system including losses, variability, testability, and performance impact (Cheng et al., 2022). Additionally, it will require ensuring that such materials are scalable, patternable, and can be purified to acceptable levels. For example, carbon nanotubes have been shown to have high performance transistors on an individual basis, but its Achilles' heel of patternability and purity remains to be resolved. It is important to recognize that for conventional computing, such devices will most likely need to be compatible with existing fabrication processes and flows, and ideally be close to drop-in complements within a silicon circuitry environment.

CMOS using polycrystalline or amorphous materials offers the promise of vertical CMOS, and in part for this reason various low (<2.5 eV) band gap oxides have been explored, such as the semiconducting oxides. There is however no acceptable p-MOSFET to date that is polycrystalline and works at device relevant doping levels. While significant theoretical and computational advances have been made in the prediction of material properties, comparatively little progress has occurred in closing the loop between prediction and synthesis and demonstrating viable new materials. Mastering polycrystalline transport will also require a concomitant understanding of electron transport in non-perfect materials—amorphous/polycrystalline/defective materials and heterointerfaces, and the physics of electron transport across heterointerfaces, such as in a small contact area. This also applies to other sources of excitations for information processing in small volumes: such as spin transport across multilayers, or interactions with phonons etc.

Memory

Today, memory is either fast, large, and expensive, as in static random-access memory (SRAM), or slow and dense, as in dynamic random-access memory (DRAM). Aside from SRAM, no other memory product on the market today is on-chip, i.e. one that can be integrated on the same chip with the logic processor to maximize speed and minimize communication distance and energy consumption. The near-perfect memory, one that is low power, as fast as SRAM, and as dense as DRAM and FLASH, and preferably with on-chip capability, does not yet exist. Identifying the materials and physics that would create such a memory is a grand challenge that would revolutionize computing. A more practical goal on a shorter time scale is to develop memories that fill in the performance/cost gaps of today's memory hierarchy such that co-design and optimization can be more effectively accomplished. Energy consumption and latency loss in accessing memory from the logic processor are emerging as major limiters of computing efficiency. The energy cost in the communications is a significant fraction of the total computing energy cost.
The relative amount of memory available for practical use is reducing due to cost and design complexity. For instance, the byte to flop ratio for high performance computing has reduced from about 1:1 possible two decades ago (Jason, 2013), to less than 1:10 today, even though a substantial part of the cost of a state-of-the art exascale computer today can be attributed to memory. Additionally, data-intensive computing workloads and the heavy demand it places upon memory intensive vector matrix multiplication have led to specialized accelerators today that have more efficient reuse of memory for computation and bring memory closer to compute, leading to compute-near-memory accelerators (Google TPU, IBM Tellum, Intel Habana, Cerebras etc.). This is done today via a combination of architecture design, heterogeneous integration and packaging. However, these will not be energy efficient enough for the large data-intensive workloads of the future and will require new approaches to matrix multiplication hardware. One of the options is "compute-in-memory" by using a Kirchoff's Law based analog step to carry out a vector dot product that nearly eliminates the shuttling of data between compute and memory through a crossbar array architecture (Haensch et al., 2022; W. Wan et al., 2022). Such a crossbar module could form a new and significant element for computing hardware, provided the right memory elements are discovered and qualified. Thinking further ahead, compute-in-memory algorithms and architectures beyond crossbar arrays can be considered, along with corresponding materials and devices for such circuits. Additionally, while relatively simplified neuron and synapse models are currently mainstream for such crossbar modules, additional device behaviors and properties, often bio-inspired, can impact the circuit in improved ways.

Heterogeneous Integration

Conventional computing has increasingly relied on the integration of specialized accelerators tightly connected to memory with the role of the CPU evolving into one of managing resources. Ideally these different processor and memory elements should be integrated onto a single silicon wafer. However, due to lithographic reticle size limitations, differences in process flows, and cost optimization, this may not be the best way forward. This has led to the emergence of heterogeneous integration, with the different chiplets (accelerators, memories etc.) grafted onto a separate carrier (typically an organic substrate, but there are different variants) and with high bandwidth, low-power interconnect links established between them—this is the direction modern computing hardware is headed. The vision for heterogeneous integration is to be able to fuse the differences between the chip and the package—i.e., achieve that same bandwidth and connectivity possible within the carrier package, as it would have if all the elements were monolithically present on a single silicon chip while significantly improving functionality. Additionally, future heterogeneous integration desires interoperability of components: the ability to create bespoke systems by mixing and matching chips and components from a set of common components and standardized interconnect links. These needs present significant challenges for fundamental materials science. These include finding a new class of organic materials (that are the substrates for the package integration) that can rival the patternability of inorganic substrates, have orders of magnitude increases in thermal conductivity over current values, and ways to fabricate and integrate electrical, photonic, and radio frequency interconnects within the substrate. There are needs for materials to engineer and reduce overall thermo-mechanical stresses to survive manufacturing processes and more importantly survive in a broad range of environmental conditions in applications, enhanced magnetic and dielectric materials for high-efficiency/low-parasitic power delivery. These materials must also be environmentally friendly and support sustainability.

Atom-scale Direct Write, 3D Nanofabrication, and Metrology

Current microelectronics is dependent upon sequential lithography driven nanofabrication, developed for two-dimensional chip architectures. It is clear that the future opportunities for microelectronics processes increasingly lies in 3D nanofabrication, including the integration of logic and memory layers stacked vertically and with dense, high bandwidth interconnects between them. Two-dimensional lithography driven processing is not optimal here. The 3D stacking of memory technologies is already a reality today. The recent demonstrations of NAND Flash memories with 232 layers (Micron, 2022) vertically stacked is a tour de force, custom engineered for a very specific device structure. This 3D stacking method may not be generally applicable to a large variety of devices. Additionally, today, current lithography techniques are limited to ~ 8 nm^3 at scale by line edge roughness and device doping processes suffer uncertainties in implant resolutions due to stochasticity. These restrictions in today's lithography driven nanofabrication sets atomic scale precision in fabrication as a challenge for the future—the ability to "write" and place features at atomic scales, and to be able to do so in three dimensions rather than two. Moreover, these methods need to be fast enough, and scalable for manufacturing. It calls for innovations in new direct write and additive synthesis methods, surface and materials chemistry innovations, and the development of systematic methodologies for widely expanding the range of selective area deposition capability available today such as atomic layer deposition and atomic layer etching.

Need for New Three-Dimensional Materials Characterization Techniques

It is likely that the significant progress achieved in dimensional scaling would have been very difficult, if not impossible, were it not for the advent of techniques that enabled one to "see" at the nanoscale. The development of near field-imaging techniques, new aberration corrected optics for electron microscopy, and improved spectroscopies (such as in medium energy ion mass scattering) through the 1980s and 1990s enabled much of microelectronics progress in the 2000s. The need for the future is in measuring three dimensional structures, preferably in a minimally disruptive manner, with atomic level chemical and structural resolution, and with rapid throughput for the next generation of microelectronics progress. Other equally important needs are in being able to observe device response while visualizing the sample at high resolutions, and with high time resolution, as well as the three-dimensional mapping of thermal characteristics of heterogeneous structures. Examples are, for instance, in observing the reaction dynamics of the memory state transition of a resistive or electrochemical random access memory device both morphologically and chemically and at sub ns timescales; or, say, measuring the 3D stress distribution variations at high resolution in a device non-destructively. If one imagines a heterogenous 3D material as a collection of pixelated voxels in high resolution, then the goal is to map each voxel against a number of characteristics that represent the thermal, electrical, stress, and chemical states of that voxel.

Need for New Thermal Materials and Understanding

Three-dimensional architectures and volumetric, rather than dispersed computing elements, allow for shorter interconnects, tighter integration of computing and memory elements, and more degrees of freedom in design. Within the current paradigm of microelectronic systems, the overarching limitation here is heat removal from three dimensional heterogeneous structures. Solving this issue calls for discovering new high thermal conductivity engineered materials and physics-based approaches for heat removal for innovations in new thermal materials and approaches. This is complementary to approach of the design of components that have extremely low energy dissipation. Additionally, the thermal physics of future heterogeneous systems, where dissimilar materials (metals, dielectrics, semiconductors) are placed at distances smaller than phonon transport lengths, requires the concomitant understanding of thermal transport in such 3D systems. This will enable the development of accurate predictive models and cooling techniques that are scalable and practical.

3 This is the half-pitch of high numerical aperture (NA) extreme ultraviolet (EUV) technology.

Processing Science

Future semiconductor manufacturing processes will need to be environmentally friendly and have stringent process targets. Looking ahead, beyond extreme ultraviolet (EUV) and high numerical aperture (NA) EUV (high NA EUV can print a half pitch of 8 nm, or equivalent to 15 silicon lattice constants), the next battleground is emerging in deposition and etching with atomic scale process control and surface control (such as the functionalization of surfaces for selective area deposition, or removal of material). At a fundamental level, we need to further understand deposition (conformality, selective deposition, creating self-aligned structures) and etching (high aspect ratio etch, no/low damage etching) and their reaction pathways. We will need to develop low temperature processing capabilities that enable many different materials to be integrated together. As device technology becomes more application-domain-specific, we will have more process technology varieties to meet specific requirements. Going forward, we may need to use different devices (device structure, device materials) to meet the system requirements.

Efficient experimental progress will need advances in theory and the simulation of material processes, particularly the simulation of non-equilibrium processes and reaction pathways for better design, predictability, and less dependence on Edisonian experimental approaches (still a large component in microelectronics materials research). As an example, in the case of a problem involving the control and prediction of etch or deposition profile upon a highly patterned surface, a coupled understanding is required at the molecular level for materials property prediction, the multiphysics of chamber processes (plasma, thermal, reaction chemistry, gas flow etc.), and the interaction of the components to predict the profiles. All of this calls for re-emphasizing research on microelectronics manufacturing processes at a fundamental level, in order to elevate semiconductor manufacturing to the next level.

Along these lines, the idea of digital twins, where one can accurately predict the trajectory of a semiconductor manufacturing process behavior, would be very important. In order to accomplish this, advancement is necessary on the computational and theory fronts, as well as tight, closed loop coupling to experiments. These developments include fundamental method development and pushing the boundaries of materials theory, in order to better understand predict properties at the molecular level, and the accurate simulation of non-equilibrium processes.

Unconventional Computing

Unconventional computing is an umbrella term for performing computing tasks outside of classical von Neumann architectures. Rethinking how computing components are put together, as well as rethinking the function of those components, allows computing to be done in completely new ways, enter new markets, and potentially address major challenges in today's computing. This is a space where research on new materials and associated devices is needed, since these new architectures do not necessarily rely on the specific properties of silicon or other conventional computing materials (e.g. copper), examples shown in Figure 3.

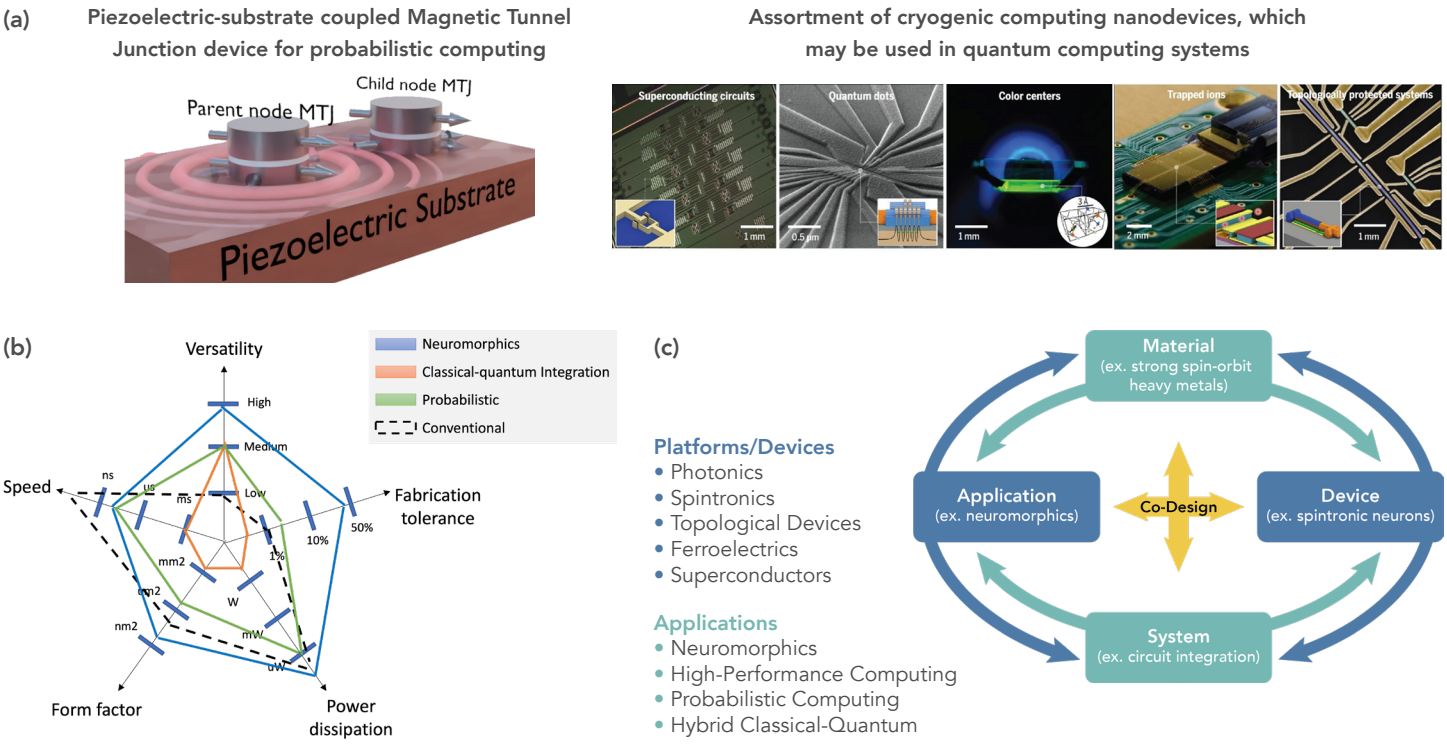

Figure 3 Unconventional Computing will require heterogenous integration of semiconductor materials, quantum, ferroelectrics, piezoelectric etc. as shown with some examples in (a) for performance improvements over conventional limits as plotted in (b). Co-Design will connect materials, devices, application, and systems with photonics, spintronics, topological devices, ferroelectrics, and superconductors. [Adapted from (Alamdar et al., 2021; Ramezani et al., 2021)]

Need for Co-Design

Let's return to the analogy in the introduction of the development of semiconductor technology over the past 50 years as akin to walking inside a tunnel. In the example of the compute function, this tunnel was refined through tight co-design between the material (silicon), device (field-effect transistor, FET), and architecture (von Neumann). In computing, co-design continues to be the key to future advancements, but the tunnel can now branch out at the exit, as new ways to compute—von Neumann or otherwise— are developed that leverage unique materials properties in smartly designed devices that are correctly fabricated to achieve system-level benefits. These benefits can include system-level energy reduction, speed-up, and/or new system-level functions and applications. This co-design is a two-way endeavor: new materials are designed into new architectures, and new applications call for new materials and devices. Take, for instance, spin-based devices where the spin of an electron is the currency for information transfer rather than charge, as in a conventional transistor. Such an approach can potentially offer advantages in the energy cost for computing, but at the expense of speed if precessional switching of the spin moment is used. Because of such a different performance envelope, spin-based devices cannot be used as a "drop-in" device, but they will require rethinking at the circuit and architecture levels, and smartly applying the benefits of the physical behavior to new use cases, in order to provide system level benefits in the computing capability.

The Compute-Energy Bottleneck

There are several critical issues in conventional computing that research in unconventional computing has been focused on addressing. A main issue is the memory bottleneck in von Neumann architectures, where the computing energy and execution time is severely limited by memory access, caused by a combination of interconnect delay (e.g. Resistor-Capacitor delay), memory latency, and above all, bandwidth. Parallel access to memory is an effective way to increase memory bandwidth. Neural network (NN) architectures, and associated materials and devices, is one way that researchers have tried to address this problem (W. Wan et al., 2020). In an artificial neural network (ANN), nodes (artificial neurons) connect to one another with different weights, and the weighted sum determines if the output of a node is above a threshold which, if so, sends that data to the next layer of the NN. NNs and associated deep learning are cornerstones of today's artificial intelligence (AI) architectures and associated applications. Compute and memory are more densely interconnected in ANNs, reducing the memory bottleneck. ANNs require different functions of their components: here, the main components are nodes (with activation functions) and weights assigned to links (synapses) between the nodes, and which can be dynamically adjusted.

Here is where research in materials and processes for microelectronics comes in. Given this very different architecture compared to the von Neumann architecture, silicon-based devices and copper-based interconnects may not be the best materials and devices for the job. The required behaviors of the components are quite different. For example, an ideal synapse for standard back-propagation training of NNs should be linear (no state-dependence on its change in weight value), symmetric (its weight value changes symmetrically for positive and negative weight updates), and controllable (can repeatably reach each weight). Other ANN architectures may have different requirements. Additionally, these should be low-energy processes, which can offer order-of-magnitude advantages over the conventional approach. This provides space for new materials research to make an impact. Key issues that research on new materials/devices for ANNs could address are the extremely high training energy and time, the difficulty of ANNs to do training and prediction in real-time, and the difficulty of ANNs to process new data and adapt quickly to new datasets, without forgetting previous data (Laborieux et al., 2021; Leonard et al., 2022). New materials and processes could usher in the vision of AI that is adaptive and immersive, with a plethora of applications in all areas of society (that also need to be ethically approached as they are enabled).

Current unconventional computing research in the space of ANNs, deep learning, and a significant component of AI research is focused on brain-inspired computing. These approaches depart from the conventional von Neumann construct of the memory-compute relation and explore new models that may blur the distinction between memory and logic. The mammalian brain is a prime example of adaptive and immersive computing, and materials and devices with brain-inspired and brain-derived functions could provide breakthroughs for AI. True progress in this field will require a concomitant increase in our understanding of brain function in living species (Martin et al., 2000).

Connecting Across the Analog-to-Digital Interface in Computing

Another critical issue being addressed with unconventional computing is the analog-to-digital-conversion (ADCs) bottleneck which is especially apparent in two areas. The first is in edge computing devices (computing done in handheld devices, internet-of-things devices, wearables, extreme environments, etc.) where the computer interacts with sensors in the real world, needs to process the data, and then send the data to the cloud. The second is for future computing designs where an analog accelerator (such as the hardware ANNs described in the previous section) will be embedded within a digital CMOS computing ecosystem, and therefore needs an analog-to-digital interface. However, ADCs are costly, can be complex, and are power hungry. For example, in analog convolutional NN accelerators, ADCs can cost about 50% of the power (Shafiee et al., 2016). Thus, the gains made by using unconventional analog computing approaches are lost in the ADC interface. Today, in-sensor computing is one way this is being addressed (T. Wan et al., 2022), as well as through new circuit building blocks such as content-addressable memories (CAMs) (Dutta et al., 2021). However, new approaches and devices are required to smoothly connect across this interface in an energy-efficient manner. This represents an opportunity for new physics-based approaches and materials.

Hybrid Systems

A third issue that unconventional computing can address is probabilistic computing and hybrid classical/quantum systems. There are many different threads to this broad-stroke area. As noted earlier, we can think of such systems as accelerators that are embedded within classical computing ecosystems. The hardware and software challenges lie in the interfacing with such accelerators. Quantum computing is based on the principles of coherence and entanglement and the loading of large classical datasets from a classical machine onto quantum bits will need new ideas, devices, and materials. In addition, quantum systems often work at low temperatures, so connecting microelectronics across different temperature regimes of operation is another potential issue. These are only some of the challenges. Quantum computing aside, naturally stochastic and probabilistic problems, such as analysis of particle physics experiments, could be more efficiently analyzed and better understood with probabilistic components (Misra et al., 2022). Stochasticity and imperfections already exist in physical systems and unconventional computing research is starting to be tuned and leveraged for these computing challenges.

Variability and Error Propagation in Low-Energy Processes

A significant benefit of digital CMOS is that the use of binary logic enables error propagation to be mitigated across a system—a value is rounded off to a zero or a one at the logic gate level and sent onwards to the next part of the circuit. Any unconventional approach that departs from digital logic needs to deal with the potential propagation and amplification of errors in a large computing system. Secondly, in keeping with the needs for low-energy computing, any new approaches will need to rely on low-energy physical or chemical processes. These can increase device variability, leading to errors. If the physical processes involved have a thermal activation component, then there is a limit to how low in energy such approaches can be selected to go. Low energy processes will be more subject to thermal fluctuations and resultant noise. These requirements can place additional burdens on the materials and physics for unconventional computing.

There are many research disciplines within each of these topics, e.g. within spintronic computing, using magnons (collective excitations of magnetic moment), spin textures (domain walls, skyrmions, etc.), and/or antiferromagnets.

The listed research trajectories face some common challenges. In predicting new materials, while machine learning (ML) can be a powerful aid, a data library of materials for ML-based "engines-of-discovery" is needed. As novel materials are developed, the physics of those materials needs to be well-understood, and the material must be successfully synthesized. New tools for metrology and measurement need to be developed and used alongside the new materials. The co-design approach of applying a new material to a new unconventional computing target is high-risk/high-reward since the requirements for actual translation to that application are astronomically stringent. There is a challenge of smartly persevering in the study of a material or device if it fails in one application, since historically the successful application is often not the first one tried. This brings in the challenge of defining success in this research endeavor, since most attempts will not make it to product. There is a major challenge of where a researcher turns when a new material or device needs to be assessed for viability in real-world applications. For those materials, devices, and processes that make it to that point, there is the challenge of scale-up and integration.

Power/High-Frequency Electronics

The need for novel active and passive components for today's power electronics cannot be overstated. With the 21st century proclaimed as the era of electrification, the need for efficient power converters is felt in almost every application. Power conversion from one level to another, or one form to another is required over a wide range of applications, from computation (1V) to the electricity grid (100's of KV). The performance, cost, and reliability metrics therefore will vary widely depending upon the applications. However, undisputedly, every fractional percent improvement in efficiency matters. The maximum impact on efficiency at low cost, can only be earned through sustainable semiconductor technologies. Development of any microelectronics technology broadly involves basic research of semiconductors, dielectrics, magnetics, and phonon transport and heat removal. Research on all these components individually or collectively will lead to efficiency improvement that can then be translated all the way to the system level. Achieving and efficient, versatile, secure, and adaptable electricity grid is just as important as an efficient, ultra-light, robust laptop with long battery life, and both are served by power electronics.

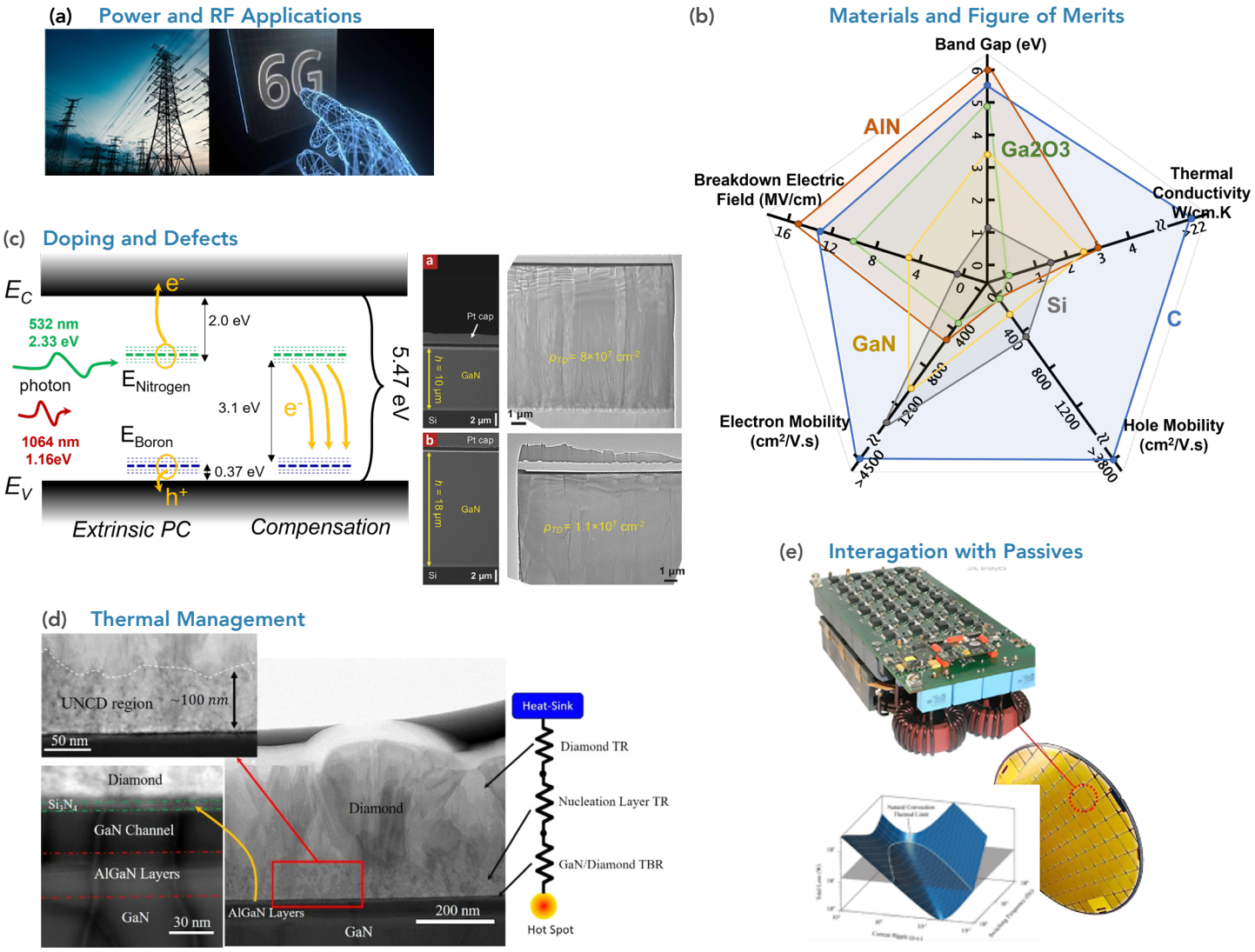

Figure 4 Power and High Frequency applications (a) will require heterogenous integration of semiconductor materials, magnetics, novel dielectrics, piezoelectric etc. for performance improvement. To reach the theoretically predicted values (b) science and technology of Doping and Defects (c), thermal management (d) and integration with passive components (e) are essential for breakthroughs. [Adapted from (Malakoutian et al., 2021; Narita et al., 2022; Tanaka et al., 2017; Tsao et al., 2018; Woo et al., 2022)]

In the case of high frequency applications (RF, 5G and beyond, THZ detection), microelectronics research is mainly driven by the need for faster, efficient, and secure communication in both defense and commercial sectors. Highly directional radar communication, long haul communication and satellite links demand new semiconductor devices and peripheral components (waveguides, interconnects, filters) that can create highly reliable, wide-band tunable, high precision, noise-free communication links and channels. These requirements boil down to basic semiconductor research to deliver high-power amplifiers at high frequencies with high-efficiency and thermal management on the transmit side. For the receive side, low-noise amplifiers with high linearity are desired.

We discuss some of the key challenges and opportunities below:

Platform for Heterogenous Integration (HI)
Similar to the case for microelectronics for computing, Heterogenous Integration, which used to be repeatedly identified as the final step in a semiconductor technology research cycle, and even delegated to higher levels of abstractions (circuit and higher) to realize, was identified as a major challenge and a technical hurdle. In the case for high-power and high frequency microelectronics, the focus for HI in this context is in exploring with basic and fundamental research towards integrating emerging semiconductors with magnetics, heat spreaders, dielectric materials, and other semiconductors for functionalities (such as logic or sensors; ultra-wide bandgap (UWBG) with WBG or with other narrow bandgap semiconductors).

Thermal Management
Similarly, thermal management was identified as a critical need for sustaining the roadmap with current and new semiconductors. Thermal management involves, but is not limited to, package-level to device-level cooling via heat sinks and heat spreaders. This involves discovery of new thermal materials (materials with a high capacity for removing or conducting away heat), growth/synthesis methods of thermal materials, and their integration. This area requires fundamental research on the synthesis, characterization, and modeling of thermal materials performance. This includes the measurement and analysis of thermal conductivities, thermal boundary resistances, integration of thermal materials, as well as theory and modeling of phonon transport in three dimensional heterostructures consisting of semiconductors, dielectrics, and metals. Eventually, this basic research needs to set platforms for electro-thermal co-design and estimate impact upon electrical performance.

Bulk Growth
Most high-power and high-frequency electronics are motivated by UWBG semiconductors. Currently some of the major challenges arise from the lack of access to substrates. Availability of low-cost, small-diameter substrates prior to scaling is a major challenge that slows the pace of research. Some of the important materials for which bulk crystal substrate development is important are aluminum nitride (AlN), boron nitride (BN), diamond, III-oxides.

Epitaxial Growth
Thin film epitaxial growth of many of the emerging active semiconductors for high-power electronics, such as Diamond, III-Oxides, and the III- (Al, Ga, In, B)—Nitrides, is poorly understood and less developed. Because of their refractory nature, they also often require extreme high temperatures for growth, and complicated deposition system design. It is important to focus on the development of epitaxial heterostructures and their control for these new materials for high-power and high-frequency applications, in the same manner that epitaxial Gallium Nitride and Silicon Carbide materials development. As has been noted for the materials research needs in the previous section, new theoretical understanding and accurate models (for instance DFT and post-DFT) are required for being able to accurately predict the properties of epitaxial films grown under non-equilibrium conditions. Property prediction of thin film materials remains at an early stage—for instance it is very difficult to accurately predict expected mobilities, and doping types in new semiconductor thin films leading to extensive trial and error experimentation. New fundamental understanding is needed of the thermodynamics and kinetics of doping and defect incorporation in wide gap semiconductors, and their electronic and defect chemistry behavior.

Dielectric Materials
UWBG materials require dielectric materials with high-K, appropriate conduction band offsets, and breakdown electric field strengths. This implies fundamental research of the synthesis and integration of dielectric materials in combination with the semiconductor material synthesis/growth/fabrication. It is critical to note that dielectric development should not be done in isolation. On-chip capacitors and other storage devices also require dielectric material studies. Synthesis, discovery, electrical characterization for their charge transport, breakdown behavior, and high field related non idealities. Studies should be targeted for the semiconductor materials that are identified as highly qualified for the applications.

Dopant and Defect Studies
With the needed expansion of the bandgap, the incorporation, activation, and compensation of both dopants and defects are not clearly understood. This can stall the development cycle of the new semiconductors, and if overlooked, can lead to major disruptions later down the line.

Magnetic, Piezoelectric, and Ferroelectric Materials
Integration of magnetic materials for on-chip inductors have been identified as a showstopper for realizing highly scaled on-chip power converters. Expansion of a piezoelectric materials base for high-Q filters that can be integrated with the semiconductor device is critical for next generation of wireless applications. Synthesis and integration of piezoelectric and ferroelectric materials, as well as their characterization, charge transport, theory, and experimental set up to characterize and model their high field behavior is needed.

Science of Processing and Characterization
Often subscribed as technology, the science of processing is a key enabler to successful technology nodes and roadmaps. Since the set of materials for active and passive components are emerging, this is a key area recognized by the panel as a research opportunity. Areas under this heading include ultra-high-pressure annealing, etching with new chemistry, high-temperature activation processes, radiation tolerance, and high-temperature behavior.

Reliability Science
Better scientific understanding of failure modes and their analysis in semiconductors is needed at earlier stages of development. Materials platforms often lack the maturity needed to make reliability science feasible. Therefore, it is crucial that innovative tools (physical and theoretical) are developed to give us an early look into the physics of degradation and failures at the device level. This will help to predict a material's full potential accurately and in a timely manner.

Research Trajectory

Based on the workshop discussions and following the descriptions of the challenges and areas of focus in the previous section, below we note eight major strategic imperatives for basic microelectronics science research. These imperatives, if met successfully, will bring sweeping changes to microelectronics (and beyond) and represent fundamental changes in the way we understand, design, or make things. Tables 1 provides an assessment of the trajectory for microelectronics materials research and its potential impact over a 5/10/20 year timeline. While this trajectory is also relevant to power electronics, we provide additional milestones for that field in Table 2. As with all scientific roadmaps and prognostications, there can be error bars that can arise from what is as-yet unknown. This trajectory should therefore be taken as an approximate guideline. We have also refrained from being overly prescriptive.

1. **Furthering the physics, chemistry, and computational science of microelectronic materials for fast and accurate predictability:** We are far from being able to predict materials properties and processes, particularly those that involve modeling non-equilibrium configurations and defective materials in the discovery science of new materials and processes. Recent progress in new computational techniques, high-performance computing and machine learning can help close this gap.
    - Digital twins and the modeling of complex materials processes across scales, from molecular levels to semiconductor processing
    - Significantly improved quantitative predictability of materials properties (doping, transport etc.) for accelerating materials discovery
    - Theory and machine learning guided materials discovery and the integration of new materials, including addressing data curation and availability of large databases for training that are broadly accessible to researchers
    - Experimentally verify results from such theory and computations (see research infrastructure discussion in later part of this report), otherwise, the theory/computation becomes an open-loop exercise without a way to assess its effectiveness. An example in the field of image understanding is the establishment of the ImageNet database. This database allows machine learning researchers to benchmark the quality of their algorithm research against a common standard and thus serves to propel algorithm research in the right direction.

2. **Atom-scale, deterministic nanofabrication in three dimensions:** With the demand for atomic scale dimensional control and for the evolution of the chip from a two- to a three-dimensional structure, the time has come to explore alternative nanofabrication methods that are scalable, exquisitely controllable, use low fabrication temperatures, reduce complexity, more amenable to three dimensional structures, and reduce reliance on stochasticity that can limit resolutions to ~1 nm in current lithography.
    - Additive and "direct-write" techniques for 3D fabrication from the atomic to the mesoscale
    - Atomic scale control of surfaces, and the development of selective area chemistries for a range of materials and deposition surfaces
    - Low-temperature fabrication techniques
    - Additive techniques at the mesoscopic scale for heterogeneous integration
    - High throughput fabrication processes because 3D fabrication would require many more process steps than conventional 2D fabrication
    - Atomic layer level etch, deposition, and functionalization control and capabilities for processing science.

3. **The physics of carrier and thermal transport in multi-scale and imperfect heterogeneous media:** As logic devices, memory devices, and interconnects scale down in size, scale up in quantity, and are assembled in three dimensionally dense and complex systems, predicting their electronic and thermal behavior becomes difficult—we lack the tools today to do so. We need a better understanding of carrier and phonon transport under these environments. These include:
    - Carrier transport in defective materials, amorphous materials, and polycrystalline materials
    - The physics of small (nanometer scale) interconnects and vias, transport across interfaces
    - Thermal physics, models, and phonon engineering for three dimensional heterogeneous environments and high-power devices
    - Physics and modeling methods that bridge atomic-scale descriptions (e.g. molecular dynamics, density functional theory) and mesoscopic descriptions that involve a large number of atoms (e.g. band theory).

4. **Three-dimensional material characterization with chemical and physical resolution at atomic scale:** Understanding and atomic level control over processes and devices can only be achieved if characterization techniques can concomitantly "keep up". There is a strong need for characterization methods that enable high chemical and structural resolution in three dimensions (few nm to sub-nm scale). While such capabilities are already emerging, these techniques should be scalable for high throughput and access, as well as be deployable in a minimally destructive manner. A second important need are in-operando, time resolved imaging techniques at high resolution that can be used during device operation, in order to study device dynamics and its relation to the materials.

5. **The science of reliability, resiliency, and adapting to the presence of noise and defects:** Defects can be a friend or a foe. The coherence properties of the nitrogen-vacancy (NV) center defect in diamond is leveraged for quantum sensing. On the other hand, defects in dielectrics lead to instability of the gate insulator and device variation and

long-term reliability issues. Noise sources in devices need to be suppressed, yet they can possibly be capitalized upon to perform probabilistic computing. Collective phenomena (e.g. coupled oscillations) and chaotic behavior are often triggered and influenced by noise sources. The role of variation at the atomic level becomes important and different from that at the several nanometer and higher scale. Fundamental studies of defects and noise may lead to new discoveries for their use to perform practical functions, in addition to contributing to a better understanding of reliability of devices.

6. **Unconventional computing approaches with a co-design perspective:** The emphasis here, which was lacking in the past, is a co-design perspective that explores new physics, materials, and harnesses dynamics within materials for computation with a strategy that includes consideration of circuits, microarchitectures, and applications for an integrated scientific approach. In this research endeavor, improved continuity of learning is needed to reach real applications that may be vastly different from the original intended application. Some clear future directions are the following:
    - New ways of connecting memory and logic in computation to overcome the memory bottleneck, such as compute-in-memory and similar approaches, and the development/exploitation of analog and multi-state memories and operations.
    - Neuromorphic and brain-inspired computing.
    - Probabilistic computing with stochastic building blocks.
    - Exploiting new physics at cryogenic temperatures (such as the spin and valley Hall effect (Li et al., 2022)) that can be harnessed for cryocomputing.
    - Exploiting new state variables (e.g. photons, spin and magnetism, topological states, other protected states, etc.) and charge-based device physics (300 mV or less without loss in off-current and gain) for extreme-efficiency computing. While individual physical phenomena often excel at the device level, it is important to bring in a system level impact viewpoint from the beginning to ensure overhead in using the devices will not outweigh its benefits.
    - Fundamental understanding of excited properties of materials or metastable states of matter that only exist under non-equilibrium conditions likely lead to ultrafast switching devices and new computational schemes (e.g. a different type of optical computing). Quantum coherence and phenomena will likely play a role in such future devices.
7. **Heterogeneous Integration:** Furthering the materials discovery science that will enable us to connect chips and chiplets seamlessly, interchangeably and at high data rates for bespoke customization. This research effort needs to include research on compatibility: how to make new materials compatible with existing systems, as well as when and how to disregard compatibility in favor of vastly different paradigms.
    - Discovery science of new classes of organic materials for packaging substrates that can have semiconductor level patternability, order of magnitude improvements in thermal conductivity compared to current materials
    - Polycrystalline and amorphous material-based transistors with performances that approach today's silicon CMOS
    - Ultralow, low-voltage non-volatile memories for digital and analog computing that are as fast as SRAM but have the density and cost profile of DRAM, and which can be integrated with logic processes
    - Integration and coupling of quantum systems to classical systems
    - Seamless power delivery: developing classes of new magnetic and dielectric materials for high efficiency, low parasitics power delivery; new approaches and devices for efficient power delivery across a range of voltages and the integration of controller and high-speed driver technology with power converters.
    - Integrating the next generation of electrical, photonic, and RF interconnects and waveguides with logic technologies, as well as high speed high frequency communications technologies
8. **Discovery science of new functional and scalable materials for high-power microelectronics components:** System performance needs are limited by what today's limited set of materials can deliver (e.g. memory, high-power electronics, substrates, interconnects, passive components etc.). A broad revitalization of research that seeks new families of scalable materials that will offer order of magnitude performance (e.g. device function, energy, footprint, cost, process temperatures, compatibility) that can also be manufactured at scale for electronics. Note: key additional material discovery needs for computing have been embedded in the other seven imperatives.
    - Jumpstart bulk crystal growth science and substrate research for homoepitaxy of high-power and high-frequency electronic devices. Will also include new synthesis processes and tools for extreme process conditions in temperatures >1200K, pressures up to GPa, and high growth rates
    - New classes of active and passive thermal materials, their synthesis, characterization of properties and their integration within heterogeneous systems to provide extreme heat removal capability for three-dimensional integration and high-power electronics
    - Ultra-wide bandgap dielectric insulators that are appropriate for wide bandgap high-power electronics. New semiconductor materials and innovations for high-power and high frequency capable of 100 kHz switching at 20 kV and 4W/mm at 1 THz
    - Research new materials for interconnects, could allow us to drive higher currents between components, faster, as well as rethink how interconnects are routed. This includes superconducting interconnects, and interconnect metallurgies that can survive high temperature, high-radiation, and chemically harsh environments (including high pressure)

Table 1. Timeline for microelectronics materials research development

Near-Term (5 years)	Mid-Term (10 Years)	Long-Term (20 Years)
Exploration and understanding of transport properties in new polycrystalline and defective materials	Polycrystalline (or amorphous) electronics begins to take shape, with practical polycrystalline logic circuits deployed for efficient computing	High quality polycrystalline electronics obviates need for single crystal materials and underlayers in many applications, leading to monolithic integrated chips
Breakthroughs in high heat conductivity and heat removal capability for thermal materials discovery	Accurate thermal physics models are well developed for heterogeneous 3D architectures; well established experimental techniques for thermal measurements for 3D structures at high resolution	Mature active and passive thermal materials integrated within 3D architectures for extreme heat removal from 3D volumes makes "volume computing" via complex 3D chip architectures with multiple logic and memory layers a working reality
Ultrafast (sub ns to ps) and fast (ns to few ns) high spatial resolution in-situ structural and chemical imaging techniques begin to enable the study of dynamic processes in reactive processes and in device behavior	Fast, minimally invasive, high throughput 4D characterization methods with high 3D resolutions are used in advanced R&D and quality control in manufacturing	
Early demonstrations of non Boolean (such as quantum, probabilistic and analog) accelerators complementing classical systems	Analysis of noise sources, adaptation foe extreme low power computing and analog approaches; leveraging noise for practical applications, including applications for probabilistic computing. Realistic ultra-low power computing systems are demonstrated that offer technology advantage. Designs inspired by neuroscience leads to better understanding and leveraging of brain-inspired properties in computing	Use of quantum, probabilistic, and neuromorphic accelerators in computing environments are routine
Demonstration of nonvolatile-based neural network crossbar arrays that compete with CMOS-based training and inference performance, while outperforming CMOS-only implementations significantly in energy efficiency	Logic devices that may use new state variables and enable sub 300 mV operation established along with demonstrated circuit/sub-system level benefits in performance/efficiency	One is able to demonstrate the devices in column B in scaled, working systems with performance and efficiency
We have now developed effective low power, fast and dense interfacing hardware strategies that interface conventional to non-conventional computing hardware (e.g. analog to digital; classical to quantum)		
	New NV memory technology (beyond SRAM, DRAM and Flash) in mass production and being broadly adopted. This includes on and off-chip memory	
Theoretical materials property prediction that is able to bridge from atomic to mesoscopic scales; implementation of physics model based reasoning in AI driven materials discovery	We are able to accurately predict material properties in non-ideal materials; able to predict reaction pathways of non-equilibrium processes; materials predictions include accurate assessment of doping and transport behavior	Accurate physics model-based AI is a success in the prediction of new materials for microelectronics; and based upon training using large, curated, publicly available datasets (as exists today for images for instance). This enables significant reduction in experimental times and Edisonian approaches to materials development and changes the way we develop materials

Near-Term (5 years)	Mid-Term (10 Years)	Long-Term (20 Years)
Additive direct write and other alternative methods to 2D lithography begin to have impact at mesoscopic to nanoscale scales for applications such as heterogeneous integration; significant progress made in selective chemistries for ALD and surface functionalization; atomic layer conformal etch and deposition processes in 3D geometries can be accurately predicted and demonstrated	Throughput for etch deposition and patterning increased by an order of magnitude. Alternative methods to lithography are in pre-manufacturing research or early manufacturing for specific applications	3D atomic scale nanofabrication is a reality: enabling atomic scale resolution and placement accuracy in three dimensions in 3D heterogeneous systems

Table 2. Timeline for additional development milestones for power electronics

Near-Term (5 years)	Mid-Term (10 Years)	Long-Term (20 Years)
Materials and scientific understanding that would enable the targeting of compact single devices that can operate at around 10kV and at around 100 kHz	Materials and scientific understanding that would enable the targeting of compact single devices that can operate at around 20kV and at around 200 kHz	At Scale for Integration (Grid)
In-situ capabilities for measurement of transport properties and structural properties	20KV Single Device at 100KHz	Control over ultra-wide band gap materials and devices, including doping, contact metallurgies, process control and nanofabrication
Thermal management informed designs that utilize new, high performance thermal materials and accurate thermal physics-based models.	Thermal physics inspired designs that include heat scavenging for other purposes	
Ready availability of new, refractory substrate and heterostructure-substrate material systems that can for high-power, high-performance devices	Ready availability of scaled up UWBGs substrates	
	Reliable Dielectric – Semiconductor interfaces	

Key Enablers to the Projected Research Trajectory

The workshop participants are enthusiastic about the project research trajectory to advance future capabilities of microelectronics. This section outlines the key enablers to realizing the projected research trajectory as targeted and coordinated infrastructure, risk management, and broader engagement with the larger research community.

Infrastructure

As noted in the previous sections, revolutionary impact in microelectronics is premised upon major progress in the discovery of new materials. We seek new capabilities, new physics-based approaches, and new understanding. At the same time, the research needs to be translational for system level impact and will require a physical scientist to plug into device and systems-level expertise—essentially also be part of co-design endeavor from systems to materials, so that basic science research is guided by translational needs in addition to the traditional curiosity-based approach. This sort of coupling has been lacking in the past for basic science research for microelectronics. Basic science for microelectronics will also require new infrastructure and access to equipment in order to target the atomic and molecular levels of control and understanding, and the design and synthesis of new materials that is necessary.

This calls for targeted and coordinated research efforts. These could be in the form of centers under one roof, or there could be other alternatives. Such capabilities would uniquely provide the materials synthesis and measurement infrastructure, teams (academia and industry), and modus operandi for research required to maximize the chances of impact.

We describe some of these infrastructure needs below. These target impact horizons typically of 15 years plus, and beyond the shorter, 5-to-10-year (or even shorter) term impact that industry related funding, and the CHIPS and Science Act proposed DoC National Semiconductor Technology Center (NSTC) targets.

We envision such coordinated efforts to be infrastructure and equipment-rich and designed for the future. Automated open data logging philosophy from experimental and simulation equipment, and its curation and availability ought to be a keystone characteristic, in order for machine learning guided materials discovery to work. Students, faculty, and industry partners would work here collectively, and research would be long term rather than based upon 3-year model where an exciting new research direction must be proposed every 2-3 years.

A. Capability for atomic scale 3D nanofabrication and process science (Research Trajectory 1, 2, 4, 7, 8): The limitations of today's two-dimensional lithography and the evolution of the chip as a three-dimensional structure sets atomic scale precision in fabrication, and in etching and deposition processes, as a challenge for the future. The goal here will be to develop these capabilities and establish the underlying science required for developing solutions. Approaches include direct write and additive methods beyond lithography, and control and prediction of reaction chemistry pathways of processes for atomic-scale selective control. Importantly this center will include a strong theory-machine learning-experimental science component that will build the understanding and capabilities for digital twins for semiconductor processes, such as deposition and etching of complex structures. It will include the capability for bespoke development of new processing methods and the associated in-situ measurement and experimental capabilities.

B. Science for next-generation microelectronic devices and their heterogeneous integration (Research Trajectory 1, 3, 5, 6, 7, 8): This research will be the focal point for establishing the fundamental understanding that may lead to new devices that will provide unprecedented performance and energy efficiency (as described earlier in this report). This would include logic, memory, power, and high-frequency devices, as well as devices that perform computation in an unconventional manner, using new physics-based approaches and new materials. Because devices must be interconnected to form a system, and heat becomes an increasingly relevant aspect of microelectronics, interconnect and thermal physics of heterogeneous systems research would be integral to this capability.

C. Capability for the discovery science of new materials for heterogeneous microelectronics (Research Trajectory 1, 2, 3, 4, 6, 7, 8): Working closely with A and B, above, this research focuses on the synthesis science of the new materials that will feed into the variety of new components necessary for heterogeneous integration and future microelectronics. This includes new materials for analog and digital memories, interconnects, high-power electronics, dielectrics, and thermal materials. Importantly it should address bulk crystal growth for high-power electronics substrates, a critical need today. We expect the study of interfaces will be integral to this Center. The research may incorporate autonomous synthesis and develop fast and accurate simulation techniques for materials discovery coupled with in-line experimentation and measurement.

D. Capability for co-design of future computation systems (Research Trajectory 3, 5, 6, 7, 8): Future systems, especially those related to non-conventional computing, must be co-designed to effectively utilize the innovations of each of the abstraction layers. Research will focus on new, long-term approaches for connecting across the analog-to-digital interface in computing, hybrid classical/quantum systems, probabilistic computing, and revisiting new ways of coupling memory and logic more efficiently. Often, researchers work mostly within one or two abstraction layers due to limitations in expertise or access to resources of other abstraction layers. This capability will bring together researchers across all abstraction layers to collaborate and share resources. Most importantly an outcome of this research will be to provide clearer, co-design informed goals for the endeavors of the other projected capabilities.

Risk Management

The process of translating new materials and processes to microelectronics application is inherently a risky endeavor. History shows that the successful application of a material, device, or technology in microelectronics industry can often be different from its initial intended application, and its application can change over time as R&D progresses. The use of low power CMOS in watches prior to their widespread use in computing, the targeting of blue light emitting injection device research for optical memory instead of their eventual utility in solid-state lighting, and the current revived interest in ferroelectric memories because of the discovery of scalable ultra-thin CMOS compatible ferroelectrics are some examples. We have noted that materials research for microelectronics is critical to continued progress in information processing efficiencies. Much of this research is basic research requiring new directions, new understanding and discovering new ways of building materials.

Two questions are important in this process: Who takes the risk? And what is considered success in this long-term research? In the workshop discussions, it was concluded that we cannot assume industry today will take the majority onus of the risk. Industry may not pivot to a new material or device unless there is a clear end-benefit. At the same time, it was concluded during the workshop that it is imperative to continue high-risk high reward type basic research for microelectronics materials if microelectronics is expected to continue on its path of remarkable impact. And the challenge then to the academia-industry-government partnership is to collectively determine how to take and manage this risk. Such research needs to be long-term focused, emphasizing fundamental and sustained understanding of relevant phenomena over gimmicky demonstrations, and be savvy to the complex interdependence of microelectronics needs in materials. *Success does not just equal successful product*: learning and next-step development are both metrics for success in such high risk-high reward endeavors.

Involving the Larger Research Community

Until now, microelectronics materials needs have been largely well-defined and set by the cadence of conventional CMOS scaling. The needs going forward however (as discussed in this report) requires a much wider array of skills and expertise than what microelectronics research has traditionally employed. The people who can define and articulate the problem statements in microelectronics materials needs are not necessary the people with the skills required to solve them. On the other hand, this latter community is often unaware or lacks a nuanced appreciation of these challenges. Opening the community up, communicating the relevant issues in a comprehensible and scientifically exciting manner, and enabling cross-pollination is key for the field. For microelectronics, this is particularly important against a backdrop of competition for research talent among a number of emerging and exciting scientific fields.

Conclusion

Microelectronics has played a major role in the historical progress of information processing and its increasing global ubiquity. Today we are at a crossroads. If research and development proceed along the current trajectory, future progress in energy efficiency and cost/compute reductions will be limited by the laws of physics in routing information at high levels of miniaturization; the memory bottleneck of the von Neuman architecture; and the need for compact, efficient, fast electronics that can handle high-power and high frequencies. Surmounting these limitations requires the theoretical and experimental exploration of new materials; new ways of fabricating and putting together heterogeneous components in three dimensions (instead of two) and at atomic scales; and the exploration of new computing architectures and new devices that can offer orders of magnitude improvement in performance, energy consumption and cost. We believe this is possible, and the preceding sections have outlined the areas of basic research in the physical sciences necessary over the next 10+ years in order to do so. The recent CHIPS and Science Act may offer an opportunity for such research, but it is important to note that for impact, the basic science research must be complemented with engineering research that informs and builds upon the basic science discoveries. This will enable the closer overlap needed between the community that recognizes the application and system level needs and issues; and the community that has the basic science skills to help accomplish the giant leaps in materials discovery science needed.

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Appendix I—Workshop Attendees

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Jean Anne Incorvia	University of Texas at Austin
Srabanti Chowdhury	Stanford University

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David Awschalom is the Liew Family Professor and Vice Dean of the Pritzker School for Molecular Engineering at the University of Chicago, a Senior Scientist at Argonne National Laboratory, and Director of the Chicago Quantum Exchange. He is also the inaugural director of Q-NEXT, one of the US Department of Energy Quantum Information Science Research Centers. Before arriving in Chicago, he was the Director of the California NanoSystems Institute and Professor of Physics, Electrical and Computer Engineering at UCSB. He served as a Research Staff and Manager at the IBM Watson Research Center. He works in spintronics and quantum information engineering, exploring the quantum states of electrons, nuclei, and photons in semiconductors and molecules with potential applications in computing, communication, and sensing. Awschalom received the APS Oliver Buckley Prize and Julius Edgar Lilienfeld Prize, the European Physical Society Europhysics Prize, the MRS David Turnbull Award and Outstanding Investigator Prize, the AAAS Newcomb Cleveland Prize, the International Magnetism Prize from the International Union of Pure and Applied Physics, and an IBM Outstanding Innovation Award. He is a member of the American Academy of Arts & Sciences, the National Academy of Science, the National Academy of Engineering, and the European Academy of Sciences.

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Dr. Ahmad Bahai, is a senior vice president and chief technology officer (CTO) of Texas Instruments responsible for guiding break-through innovation, corporate research and Kilby Labs. Dr. Bahai is an Adjunct professor at Stanford University, and IEEE Fellow. He was a professor in residence at UC Berkeley from 2001-2010. Throughout his career, Dr. Bahai has held a number of leadership roles including director of research labs and chief technology officer of National Semiconductor, technical manager of a research group at Bell Laboratories and founder of Algorex, a communication and acoustic IC and system company, which was acquired by National Semiconductor. He holds a Master of Science in Electrical Engineering from Imperial College, University of London and a doctorate degree in Electrical Engineering from University of California, Berkeley.

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Kerem Camsari received his PhD in Electrical and Computer Engineering from Purdue University in 2015, where he continued on as a post-doctoral researcher between 2015 and 2020 before joining the department of Electrical and Computer Engineering in UC Santa Barbara in 2020. His PhD work established a modular approach to connect a growing set of emerging materials and phenomena to circuits and systems, a framework that has also been adopted by others. Later, he used this approach to establish the concept of p-bits and p-circuits as a bridge between classical and quantum circuits to design efficient, domain-specific hardware accelerators in the beyond-More era of electronics. His work has been published in many refereed journals and conferences including Nature, Nature Electronics, Science Advances, Physical Review X. He is a founding member of the Technical Committee on Quantum, Neuromorphic and Unconventional Computing within the IEEE Nanotechnology Council where he leads the unconventional computing section. He has received the IEEE Magnetics Society Early Career Award and an Office of Naval Research Young Investigator Award for his work on probabilistic computing. He is a senior member of the IEEE.

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Supratik is a Professor at the Pritzker School of Molecular Engineering, and holds a joint appointment as a scientist and strategy advisor at Argonne National Labs. Earlier, till 2015 he worked at IBM Research where he last served as the Director of Physical Sciences. He research is in the area of new materials for future information processing systems.

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Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He has been exploring new packaging paradigms and device innovations that may enable wafer-scale architectures, in-memory analog compute and medical engineering applications. He is a fellow of IEEE, APS, iMAPS and NAI as well as a Distinguished Lecturer of IEEE EDS and EPS. He is on the Board of Governors of IEEE EPS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012 and the 2020 iMAPS Daniel C. Hughes Jr Memorial award and the iMAPS distinguished educator award in 2021.

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Debdeep Jena is the David E. Burr Professor of Engineering at Cornell University. He is in the departments of Electrical and Computer Engineering and Materials Science and Engineering, and is a field member in the department of Applied and Engineering Physics. He joined Cornell in 2015 from the faculty at Notre Dame where he was since August 2003, shortly after earning the Ph.D. in Electrical and Computer Engineering from the University of California, Santa Barbara (UCSB). His teaching and research are in the quantum physics of semiconductors and electronic and photonic devices based on quantized semiconductor structures (e.g. Nitrides, Oxides, 2D Materials), and their heterostructures with superconductors, ferroelectrics and magnets, with device applications in energy-efficient transistors, light-emitting diodes and RF and power electronics and quantum computation and communications. His research is driven by the goal to enable orders of magnitude increase in the energy efficiency and speed for computation, memory, communications, lighting, and electrical energy management ranging from the chip to the grid. The research from his group has been published in more than 300 journal papers including in Science, Nature, Physical Review Letters, Applied Physics Letters and Electron Device Letters. Several patents have been granted for the groups research work. He is a fellow of the American Physical Society and is the winner of teaching awards and research awards such as the ISCS young scientist award in 2012, MBE young scientist award in 2014, and awards from the industry such as the IBM faculty award in 2012, and most recently the Intel Outstanding Research award in 2020.

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Haitong Li is an incoming Assistant Professor of Electrical and Computer Engineering at Purdue University. He received Ph.D. and M.S. in Electrical Engineering from Stanford University, and B.S. in Microelectronics from Peking University. His research interests are in the new device technologies and circuit designs for energy-efficient computing, and nanotechnology-inspired artificial intelligence hardware. Haitong serves as a committee member for the IEEE Electron Devices Society (EDS) VLSI Technology and Circuits Committee, and has held research positions at Meta Reality Labs and Arm Research. He is a recipient of 2019 IEEE EDS PhD Student Fellowship and 2016 IEEE EDS Masters Student Fellowship.

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Mark Lundstrom is the Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering at Purdue University in West Lafayette, Indiana, U.S.A. He received his Ph.D. from Purdue in 1980 and BEE and MSEE degrees from the University of Minnesota in 1973 and 1974. Between his MS and Ph.D. degrees, he worked at Hewlett-Packard Corporation on integrated circuit process development and manufacturing. At Purdue, his research has focused on semiconductor devices, the physics of electronic, thermal, and electro-thermal carrier transport, and modeling and numerical simulation. His contributions to nanoelectronics have been recognized by the Semiconductor Research Corporations Technical Excellence Award, the Semiconductor Industry Associations University Research Award, and the IEEE Cledo Brunetti Award. Lundstrom is also known for his contributions to education, which have been recognized by the ASEE Frederick Emmons Terman Award, the IEEE Electron Device Society Education Award, the SRC Aristotle Award, and the 2018 IEEE Leon K. Kirchmayer Graduate Teaching Award. He is the author of four textbooks on carrier transport and semiconductor devices. Lundstrom was the founding director of the Network for Computational Nanotechnology, which created the nanoHUB.org science gateway, a major online resource for nanoelectronic materials and devices. Dr. Lundstrom is a Life Fellow of the IEEE, and fellow of the American Physical Society and American Association for the Advancement of Science, and a member of the U.S. National Academy of Engineering.

Ravi Mahajan, Intel Fellow
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Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives. He has led Pathfinding efforts to define Package Architectures, Technologies and Assembly Processes for multiple Intel silicon nodes including 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Ravi joined Intel in 1992 after earning his Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intels EMIB technology. His early insights have led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques for thermo-mechanical stress model validation. His contributions during his Intel career have earned him numerous industry honors, including the SRCs 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 Outstanding Service and Leadership to the IEEE Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award and the 2020 ASME EPPD Excellence in Mechanics Award. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He has long been associated with ASMEs InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was elected to the National Academy of Engineering in 2022 for contributions to advanced microelectronics packaging architectures and their thermal management.

Theresa Mayer, Executive VP for Research and Partnerships
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Theresa S. Mayer is the executive vice president for research and partnerships at Purdue University, where she oversees the institutions $690 million research enterprise and supports holistic engagements with federal, industry, and global strategic partners. Previously, in her roles leading research and innovation efforts at Virginia Tech and Penn State University, Mayer was instrumental in creating collaborative and cutting-edge research ecosystems that engaged industry and enhanced regional economic development. She is widely recognized for her work in advanced manufacturing of nanoscale electronic, optical, and biomedical devices, which has been supported by the NSF, DOD, DOE, NIH, and industry. Mayer has over 350 technical publications, invited presentations and tutorials, and holds ten patents in these areas. She served on the U.S. Presidents Council of Advisors on Science and Technology and is a fellow of the Institute for Electrical and Electronics Engineers.

Umesh Mishra, Professor
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Professor Mishra joined ECE Department at the University of California, Santa Barbara in 1990 from the Department of Electrical and Computer Engineering at North Carolina State University. A recognized leader in the area of high-speed field effect transistors, Dr. Mishra has made major contributions at every laboratory and academic institution for which he has worked, including Hughes Research Laboratories in Malibu, California; the University of Michigan at Ann Arbor; and General Electric, Syracuse, New York. His current research areas attempt to develop an understanding of novel materials and extend them into applications. He is the Director of the AFOSR PRET Center for Non-Stoichiometric Semiconductors and of the ONR MURI Center (IMPACT), which relates to the application of SiC and GaN based transistors for power amplification.

Uday Mitra, Vice President, Technology Roadmap & Strategy
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Dr. Mitra is Vice President, Technology Roadmap and Strategy at Applied Materials. He has nearly 4 decades of experience in the industry managing technology integration, lithography, etch, thin films and packaging modules for both logic and memory products. Prior to joining Applied in 2005, he was director of technology integration at Intel Corporation, where he spent 17 years holding various management positions. Uday received his B. Tech from IIT, Bombay and Ph.D. in Materials Science from MIT and is a recipient of the Henry Marion Howe Medal from the American Society of Materials International.

Vijay Narayanan, IBM Fellow and Senior Manager
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Dr. Narayanan received his B.Tech. in Metallurgical Engineering from the Indian Institute of Technology, Madras (1995), and his M.S. (1996) and Ph.D. (1999) in Materials Science and Engineering from Carnegie Mellon University. After completing post-doctoral research at Arizona State University, Dr. Narayanan joined the IBM T. J. Watson Research Center in 2001 where he pioneered High-ï« /Metal Gate Research and Development from the early stages of materials discovery to development and implementation in manufacturing. These High /Metal Gate materials form the basis of all recent IBM systems processors and of most low-power chips for mobile devices. Currently, Dr. Narayanan is an IBM Fellow and Senior Manager at IBM Research where he is the strategist for Physics of AI and leads a worldwide IBM team developing Analog Accelerators for AI applications within the IBM Research AI Hardware Center. Dr. Narayanan is an IEEE Senior Member and was elected a Fellow of the American Physical Society in 2011. He is an author of over 100 journal and conference papers, holds more than 230 US patents, and has edited one book: Thin Films On Silicon: Electronic And Photonic Applications.

Amanda Petford-Long, Director, Materials Science Division
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Amanda Petford-Long is an Argonne Distinguished Fellow in the Materials Science Division (MSD) at Argonne National Laboratory in Chicago. In addition to her own research program, she serves as the Division Director of MSD and leads Argonne's Microelectronics strategy development group. She has a D.Phil (PhD) in Materials Science from the University of Oxford and a B.Sc in Physics from University College, London. She moved to Argonne in 2005 from the University of Oxford where she was a full professor in the Materials Department. Her research focuses on nanomaterials and a particular emphasis is on magnetic and resistive-switching nanostructures with potential applications in information storage technology, and on the use of in-situ TEM. She has published over 350 scientific papers. She is a Fellow of the Royal Academy of Engineering, the Royal Microscopical Society, and the American Physical Society and is a Professor in the Materials Science and Engineering Department at Northwestern University.

Dan Radack, Assistant Director
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Daniel Radack is Assistant Director in the Information Technology and Systems Division at the Institute for Defense Analyses (IDA) where he analyzes and seeks solutions to the US Government's problems related to microelectronics. From 1998 to 2008, he was with DARPA where he started a portfolio of R&D programs that advanced high performance semiconductor technologies for defense and national security applications, providing foundational advances to the state of art in Silicon-Germanium, Silicon-on-Insulator, radiation hardening, platform-based design, multi-chip packaging, and heterogeneous integration/3D integration. Before that, he worked in the defense electronics industry and for NIST where he studied dynamic test circuits and semiconductor metrology. He has a BS, MS, and Ph.D. in electrical engineering from the University of Maryland. He is a Fellow of the IEEE.

Chris Richardson, Research Scientist
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Christopher J.K. Richardson is a research scientist at the Laboratory for Physical Sciences, deputy director of the LPS Qubit Collaboratory, and an adjunct professor in the Department of Materials Science and Engineering at the University of Maryland. He received his PhD and MS degrees in materials science and engineering from Johns Hopkins University and his BS degree in engineering physics from the University of Maine. He has authored papers and conference contributions in technical areas spanning epitaxial material design, growth, materials characterization, optoelectronic devices, and superconductor resonators. His current research interests include molecular beam epitaxy of dissimilar materials and the materials science of quantum computing.

Sayeef Salahuddin, Professor
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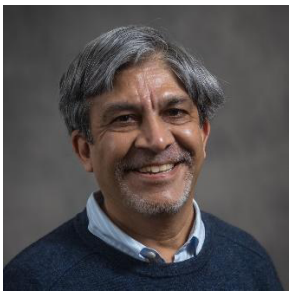
S. Salahuddin is the TSMC Distinguished Professor of Electrical Engineering and Computer Sciences at the University of California Berkeley. His work has focused mostly on conceptualization and exploration of novel physics for low power electronic and spintronic devices. Salahuddin received the Presidential Early Career Award for Scientist and Engineers (PECASE) from President Obama. Salahuddin also received a number of other awards including the National Science Foundation CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the Airforce Office of Scientific Research and the Army Research Office, and the IEEE George E Smith Award. Salahuddin is a co-director of the Berkeley Device Modeling Center (BDMC) and Berkeley Center for Negative Capacitance Transistors (BCNCT). Salahuddin is also a co-director of ASCENT, which is a flagship device technology effort in the US, jointly supported by SRC and DARPA. He served on the editorial board of IEEE Electron Devices Letters (2013-16) and was the chair the IEEE Electron Devices Society committee on Nanotechnology (2014-16). Salahuddin is a Fellow of the IEEE and the APS.



Nitin Samarth, Professor
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Dr. Samarth is Downsbrough Department Head and Professor of Physics at Penn State University. He obtained an undergraduate degree in physics from IIT Bombay and a Ph.D. in physics from Purdue University. He joined the physics faculty at Penn State in 1992 after work as a post-doctoral research associate and research faculty fellow at the University of Notre Dame. Dr. Samarth has pioneered the epitaxial synthesis of a variety of spin-based quantum materials, resulting in fundamental advances in our understanding of semiconductor spintronics, nanomagnetism, topological materials, and quantum information. He is a Fellow of the American Physical Society, Fellow of the American Association for the Advancement of Science, and a recipient of Penn State's Faculty Scholar Medal in the Physical Sciences and Penn State's George Atherton Excellence in Teaching Award. He also received an Outstanding Physics Alumnus Award from Purdue University and an Outstanding Alumnus Award from IIT Bombay. He has served on the elected chair-line of the Division of Materials Physics of the American Physical Society.

Darrell Schlom, Professor
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Darrell Schlom is the Herbert Fisk Johnson Professor of Industrial Chemistry in the Department of Materials Science and Engineering at Cornell University. He also holds an honorary affiliation as the first Leibniz Chair of the Leibniz- Institut Kristallzüchtung (IKZ) in Berlin, Germany. After receiving a B.S. degree from Caltech and a Ph.D. from Stanford University, he was a post-doc at IBMs research lab in Zurich, Switzerland. His research involves the heteroepitaxial growth and characterization of oxide thin films by reactive molecular-beam epitaxy (MBE), especially utilizing a materials-by-design approach to discover materials with properties superior to any known. His work on materials synthesis enabling materials discovery has been recognized by the MRS Medal from the Materials Research Society, the Frank Prize from the International Organization for Crystal Growth, the McGroddy Prize from the American Physical Society, and the John A. Thornton Memorial Award/Lecture from the American Vacuum Society. He is a Fellow of the American Physical Society, the Materials Research Society, the American Vacuum Society, and is a member of the National Academy of Engineering.

Susanne Stemmer, Professor
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Susanne Stemmer is Professor of Materials at the University of California, Santa Barbara. She did her doctoral work at the Max-Planck Institute for Metals Research in Stuttgart (Germany) and received her degree from the University of Stuttgart in 1995. Her research interests are in the development of scanning transmission electron microscopy techniques, molecular beam epitaxy of novel materials, strongly correlated oxide heterostructures, and topological matter. She has authored or co-authored about 300 publications. Honors include election to Fellow of the American Ceramic Society, Fellow of the American Physical Society, Fellow of the Materials Research Society, Fellow of the Microscopy Society of America, and a Vannevar Bush Faculty Fellowship of the Department of Defense.

H.S. Philip Wong, Professor, Co-Chair
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H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering at Stanford University. He joined Stanford University as Professor of Electrical Engineering in 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. From 2018 to 2020, he was on leave from Stanford and was the Vice President of Corporate Research at TSMC, the largest semiconductor foundry in the world, and since 2020 remains the Chief Scientist of TSMC in a consulting, advisory role. He is a Fellow of the IEEE and received the IEEE Electron Devices Society J.J. Ebers Award, the society's highest honor to recognize outstanding technical contributions to the field of electron devices that have made a lasting impact, as well as the IEEE Andrew S. Grove Award, the IEEE Technical Field Award to honor individuals for outstanding contributions to solid-state devices and technology. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems, the faculty director of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI), and the faculty director of the Stanford Nanofabrication Facility.

Appendix II—Workshop Agenda and Prospectus

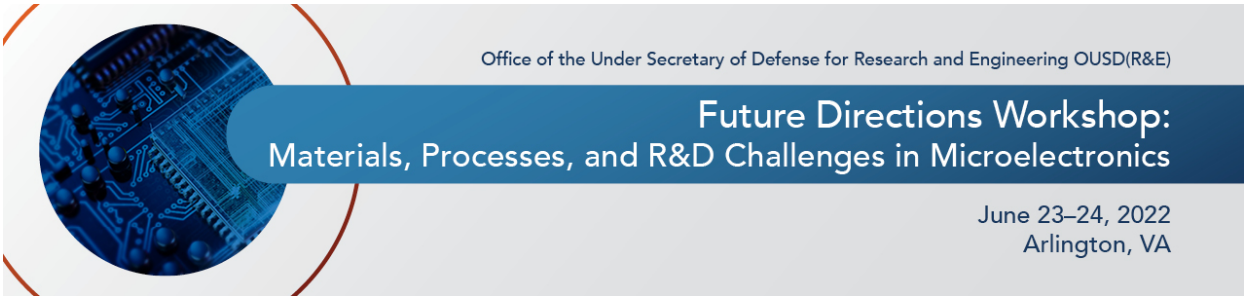
Basic Research Innovation Collaboration Center
4100 N. Fairfax Rd. | Fourth Floor| Suite 450
Arlington, VA 22203

DAY 1—THURSDAY, June 23, 2022

Time	Title	Speaker
8:00—8:10	Check-in and Continental Breakfast	
8:10 - 8:20	Welcome, Introductions and Expectations	Supratik Guha, U Chicago & Argonne National Laboratories Dr. Bindu Nair, OUSD(R&E)/BRO
8:20 - 8:50	Plenary Talks	Ravi Mahajan, Intel Uday Mitra, Applied Materials
8:50—9:00	Breakout Instructions and Morning Break	
9:00—10:45	Working Group I: Define the Problem *Small group discussions to frame a vision for future of microelectronics and identify the greatest hurdles to achieving it.* Group A –Conventional Computing Group B—Unconventional Computing Group C—Power and High Frequency Electronics	
10:45—11:00	BREAK - *Transition to main conference room and leads prepare outbriefing*	
11:00 –12:00	Working Group 1: Outbriefing	
12:00—1:00	LUNCH (provided for participants)	
1:00—2:45	Working Group II: Technical Capabilities and Opportunities *What are the promising research directions for microelectronics? What are the potential capabilities in the 10- to 20-year horizon?* Group A –Conventional Computing Group B—Unconventional Computing Group C—Power and High Frequency Electronics	
2:45—3:00	BREAK - *Transition to main room and leads prepare outbriefing*	
3:00—3:45	Working Group II: Outbriefing	
3:45—4:45	Whole Group Discussion on Key Programmatic/Infrastructure Insights	
4:45—5:00	Summary of Day	Co-chairs
5:00	MEETING ADJOURNED FOR THE DAY	

DAY 2—FRIDAY, June 24, 2022

Time	Title	Speaker
8:00—8:15	Check-in and Continental Breakfast	
8:15—8:30	Welcome and Day 1 Recap	Co-chairs
8:30—9:00	What's Missing?	
9:00 - 9:15	Plenary Talk	Ahmad Bahai, Texas Instruments
9:15 -10:15	**Programmatics Discussion** Whole group discussion on key programmatic hurdles and opportunities.	
10:15—10:30	BREAK	
10:30—11:30	**Infrastructure Discussion** Whole group discussion on key infrastructure hurdles and opportunities.	
11:30—11:45	Discussion of Key Ideas/Components for Report	
11:45—12:00	Closing Remarks Co-chairs	
12:00	DEPARTURE	



Co-Chairs: Supratik Guha (University of Chicago and Argonne National Laboratory), H.-S. Philip Wong (Stanford University), Jean Anne Incorvia (University of Texas at Austin)

Microelectronics is a complex field with ever-evolving technologies and business needs, fueled by decades of continued fundamental materials science and engineering advancement. Decades of dimensional scaling have led to the point where even the name "microelectronics" inadequately describes the field, as most modern devices operate on the nanometer scale. As we reach physical limits and seek more efficient ways for computing, research in new materials may offer alternative design approaches that involve much more that electron transport (e.g. photonics, spintronics, topological materials, and a variety of exotic quasi-particles). New engineering processes and capabilities offer the means to take advantage of new materials designs (e.g. 3D integration, atomic scale fabrication processes and metrologies, digital twins for semiconductor processes and microarchitectures). The wide range of potential technological approaches provides both opportunities and challenges, as technology roadmaps must be drawn, and investment decisions must be made. A forward-looking research program therefore needs to be uniquely suited and nuanced in response to the complexities of the field.

This Future Directions Workshop on Materials, Processes, and R&D Challenges in Microelectronics, sponsored by the Basic Research Office in the Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)), aims to identify the key drivers, requirements, challenges, and essential basic research questions to enable future generations of microelectronics. The goal of the workshop is to address the following question:

> Given the state of research and developments in the overall field of microelectronics, how might future research programs in materials and processes be modified to further enhance impact to technology?

In doing so, the panel will take a fresh look at microelectronics research and business needs, the current role of academia, government and industry, and their respective strengths and weaknesses. What has worked well so far in the current structure of microelectronics materials research and what could be improved upon? Based upon these, the panel will provide recommendations for technical areas of emphasis, funding models, metrics, and incentive frameworks that could inform a new way of structuring microelectronics research programs. These will take into account materials and processes research implications considering the uncertainties, basic science challenges, engineering pull, scale-up issues, etc.

This Future Directions workshop will gather leaders from across academia, industry, and government to consider three aspects of the microelectronics field:

Materials, Devices, Processes, and Metrologies

- What are the most promising materials-focused research areas? This includes evaluation (without being over prescriptive) of the technical areas of emphasis that will be important going forward, including research needs in supporting infrastructure and supply chain.
- How might materials research better connect with devices and applications? It would be important to be informed by the entire co-design space of microelectronics research in this workshop since algorithms and architectures drive the research propositions downstream, and the approach to the design-to-device process is changing.
- What are the needs in both existing areas of major impact (server-based computing, mobile computing, and next-G communications), as well as areas for future expansion (smart/electric vehicles, for example)?

Programmatic

- What should be the goals of materials-focused research? What should be the metrics for research output?
- What incentive structures should be put in place, including those that may require stakeholders to be displaced out of traditional comfort zones?
- What evaluation criteria are needed?
- What organizational structures (federal research programs) provide the maximum benefits in speed, flexibility, resiliency, and creativity? How can accountability be ensured, without stifling creativity or preventing high risk, high reward efforts?
- What is the time horizon for academic research impact? What type of research should be funded, and what should not be funded? By what criteria and when is it decided to continue, pause, or discard approaches? What should be different from the way this is done today?

Academia-Industry-Government Partnerships

- What are the unique strengths and weaknesses of industry and academia? How are they interacting and leveraging each other's strengths? What is the optimal balance of responsibilities and investments? What are the incentives to consider?
- How can we further leverage the strengths and capabilities of the national labs for microelectronics materials research?
- What can be gained from potential international partners and how? What are the opportunities and roadblocks? What policies must be changed or put in place?

A key outcome of this Workshop will be a roadmap of basic science research needs that, if addressed in the next 10-20 years, can substantially advance future microelectronics. Materials, devices, processes, and metrologies are the focal point for this workshop. These are areas in which the US is at considerable risk of falling behind and needs to stay strong to remain a key player. The discussions and ensuing distributed report will provide valuable long-term guidance to the DoD community, as well as the broader federal funding community, federal labs, and other stakeholders. Workshop attendees will emerge with a better ability to identify and seize potential opportunities in the different fields addressed.